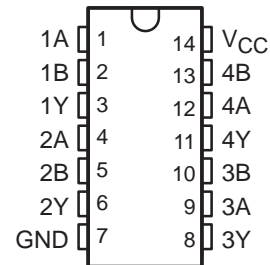


# SN74HC132-Q1 QUADRUPLE POSITIVE-NAND GATE WITH SCHMITT-TRIGGER INPUTS

SCLS553 – JANUARY 2004

- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 40- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 14$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Operation From Very Slow Input Transitions
- Temperature-Compensated Threshold Levels
- High Noise Immunity
- Same Pinouts as 'HC00

D OR PW PACKAGE  
(TOP VIEW)



† Contact factory for details. Q100 qualification data available on request.

## description/ordering information

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The SN74HC132 performs the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

This circuit is temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SOIC – D	Reel of 2500		
–40°C to 125°C	SOIC – D	Reel of 2500	SN74HC132QDRQ1	HC132Q1
	TSSOP – PW	Reel of 2000	SN74HC132QPWRQ1	HC132Q1

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT Y
A	B	
H	H	L
L	X	H
X	L	H



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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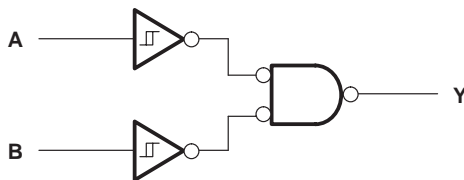
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# SN74HC132-Q1

## QUADRUPLE POSITIVE-NAND GATE WITH SCHMITT-TRIGGER INPUTS

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### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package .....	86°C/W
..... PW package .....	113°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 6$ V	4.2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V		0.5	V
		$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 6$ V		1.8	
$V_I$	Input voltage	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	V
$T_A$	Operating free-air temperature	-40		125	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**SN74HC132-Q1**  
**QUADRUPLE POSITIVE-NAND GATE**  
**WITH SCHMITT-TRIGGER INPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V <sub>T+</sub>			2 V	0.7	1.2	1.5	0.7	1.5	V
			4.5 V	1.55	2.5	3.15	1.55	3.15	
			6 V	2.1	3.3	4.2	2.1	4.2	
V <sub>T-</sub>			2 V	0.3	0.6	1	0.3	1	V
			4.5 V	0.9	1.6	2.45	0.9	2.45	
			6 V	1.2	2	3.2	1.2	3.2	
V <sub>T+</sub> - V <sub>T-</sub>			2 V	0.2	0.6	1.2	0.2	1.2	V
			4.5 V	0.4	0.9	2.1	0.4	2.1	
			6 V	0.5	1.3	2.5	0.5	2.5	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9	V	
			4.5 V	4.4	4.499		4.4		
			6 V	5.9	5.999		5.9		
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3		3.7		
		I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8		5.2		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1	V
			4.5 V		0.001	0.1		0.1	
			6 V		0.001	0.1		0.1	
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4	
		I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0,	I <sub>O</sub> = 0	6 V			2		40	μA
C <sub>i</sub>			2 V to 6 V		3	10		10	pF

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>pd</sub>	A or B	Y	2 V		60	120		186	ns
			4.5 V		18	25		37	
			6 V		14	21		32	
t <sub>t</sub>		Any	2 V		28	75		110	ns
			4.5 V		8	15		22	
			6 V		6	13		19	

operating characteristics, T<sub>A</sub> = 25°C

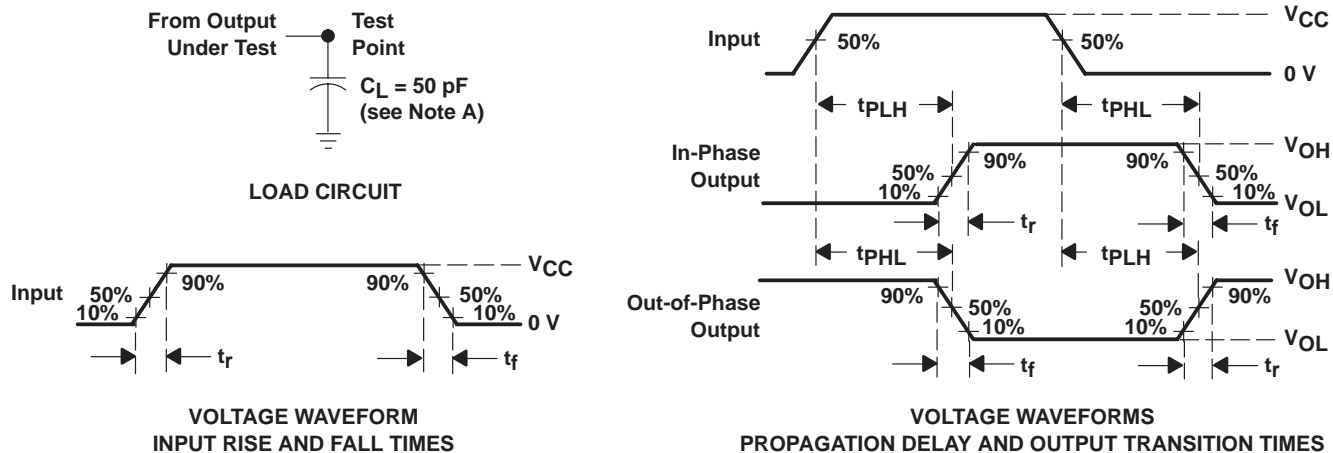
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per gate	No load	20	pF



# SN74HC132-Q1 QUADRUPLE POSITIVE-NAND GATE WITH SCHMITT-TRIGGER INPUTS

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## PARAMETER MEASUREMENT INFORMATION

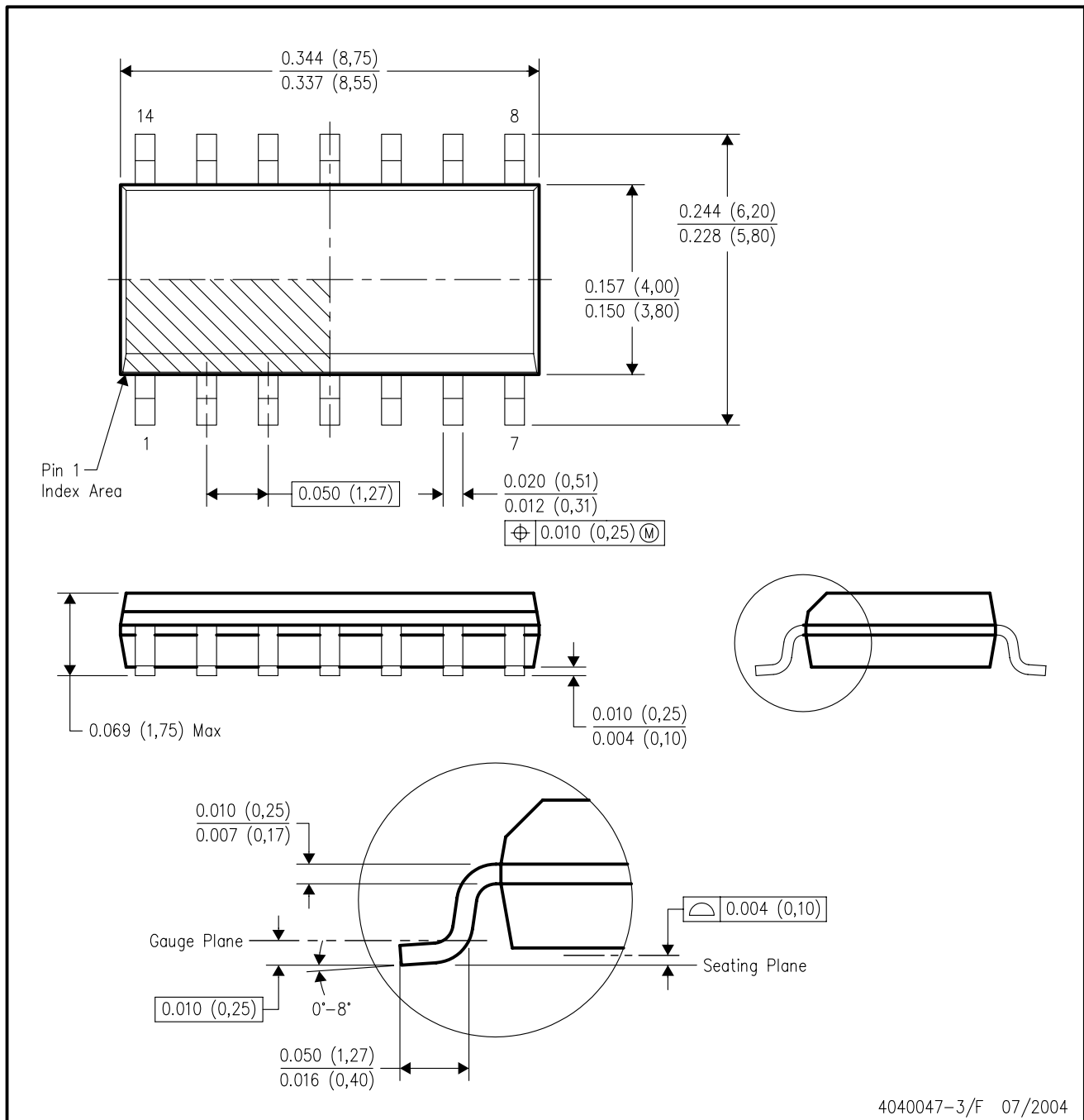


- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - C. The outputs are measured one at a time with one input transition per measurement.
  - D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE

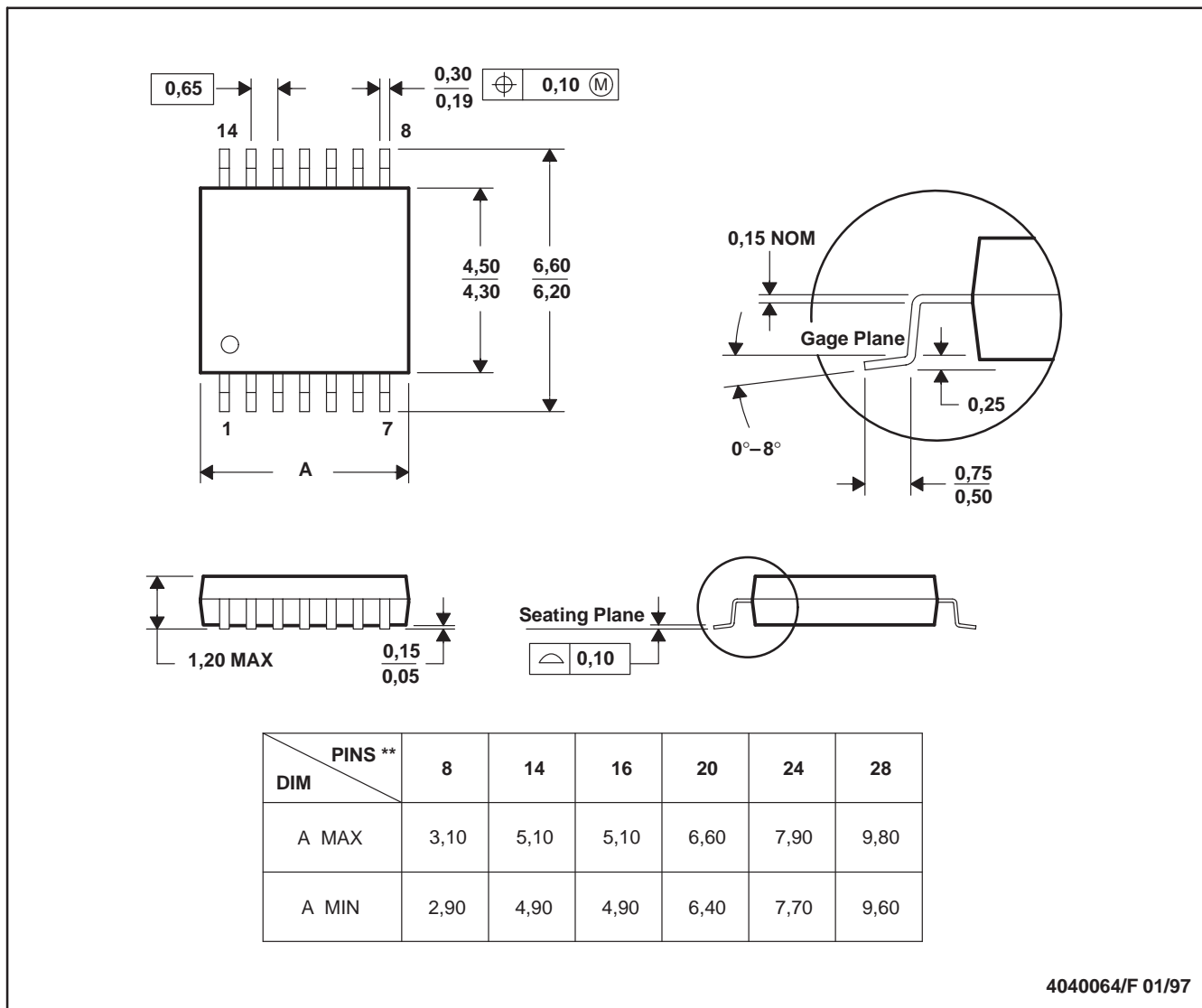


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AB.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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