National Semiconductor

February 1995

LMC835 Digital Controlled Graphic Equalizer

General Description

The LMC835 is a monolithic, digitally-controlled graphic equalizer CMOS LSI for Hi-Fi audio. The LMC835 consists of a Logic section and a Signal Path section made of analog switches and thin-film silicon-chromium resistor networks. The LMC835 is used with external resonator circuits to make a stereo equalizer with seven bands, ±12 dB or ±6 dB gain range and 25 steps each. Only three digital inputs are needed to control the equalization. The LMC835 makes it easy to build a μP-controlled equalizer.

The signal path is designed for very low noise and distortion, resulting in very high performance, compatible with PCM audio.

Features

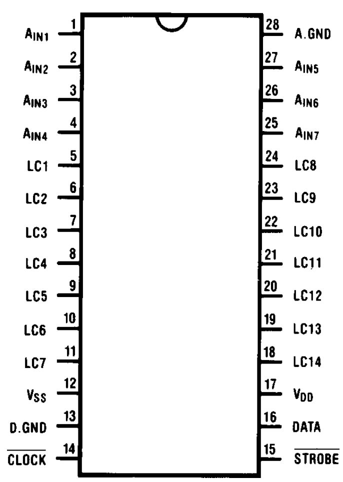
- No volume controls required
- Three-wire interface
- 14 bands, 25 steps each
- ±12 dB or ±6 dB gain ranges
- Low noise and distortion
- TTL, CMOS logic compatible

Applications

- Hi-Fi equalizer
- Receiver
- Car stereo
- Musical instrument
- Tape equalization
- Mixer
- Volume controller

Connection Diagrams

Dual-In-Line Package

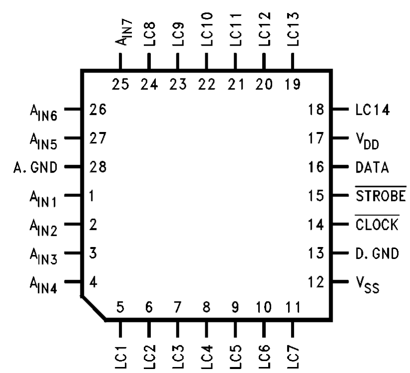


TL/H/6753–1

Top View

Order Number LMC835N
See NS Package N28B

Molded Chip Carrier Package

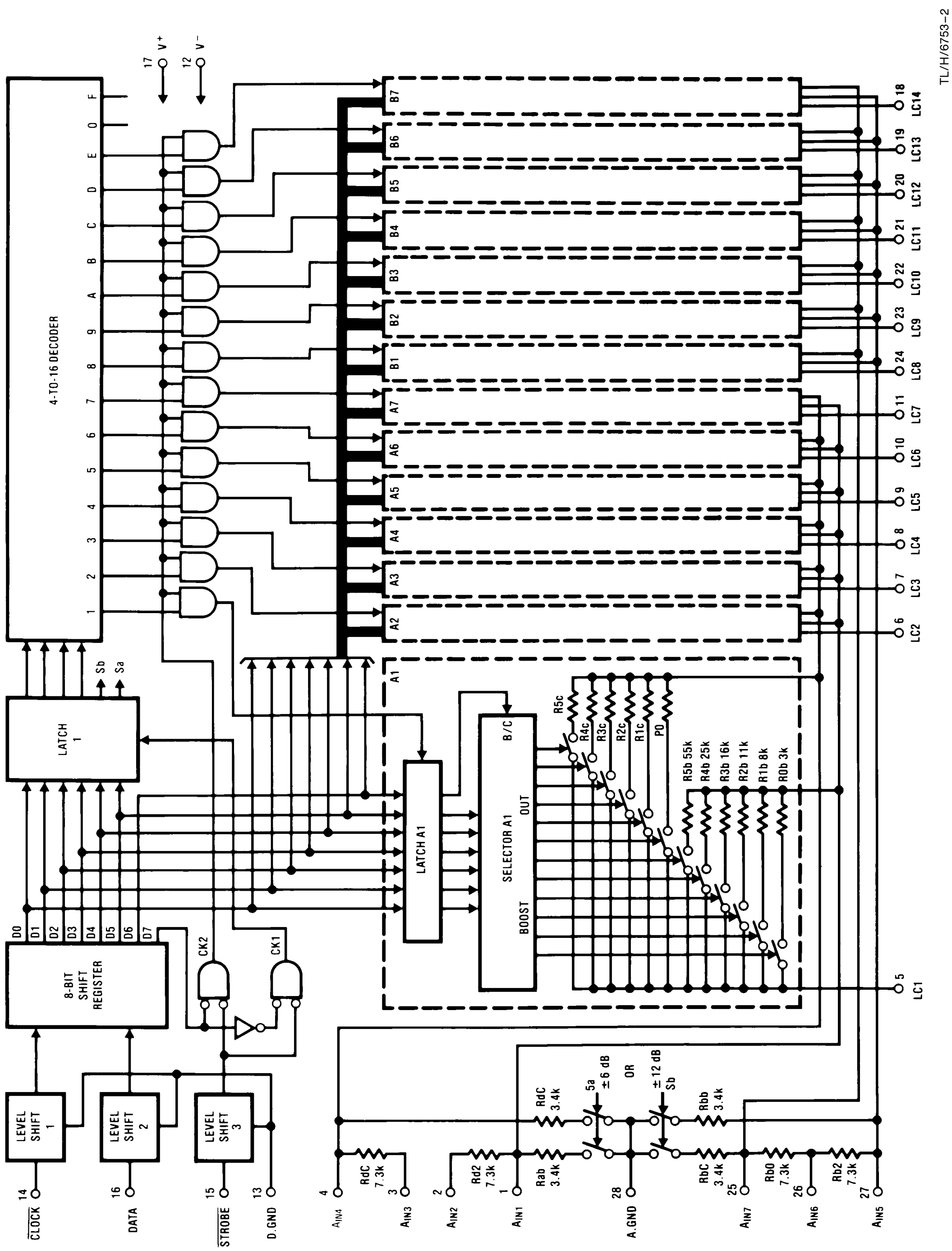


TL/H/6753–26

Top View

Order Number LMC835V
See NS Package V28A

Block Diagram



Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, $V_{DD}-V_{SS}$	18V
Allowable Input Voltage (Note 1)	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Storage Temperature, T_{stg}	$-60°C$ to $+150°C$
Lead Temperature (Soldering, 10 sec), N Pkg	$+260°C$
Lead Temperature, V Pkg	
Vapor Phase (60 sec)	$+215°C$
Infrared (15 sec)	$+220°C$

Operating Ratings

Supply Voltage, $V_{DD}-V_{SS}$	5V to 16V
Digital Ground (Pin 13)	V_{SS} to V_{DD}
Digital Input (Pins 14, 15, 16)	V_{SS} to V_{DD}
Analog Input (Pins 1, 2, 3, 4, 25, 26, 27) (Note 1)	V_{SS} to V_{DD}
Operating Temperature, T_{opr}	$-40°C$ to $+85°C$

Electrical Characteristics (Note 2) $V_{DD}=7.5V$, $V_{SS}=-7.5V$, A.GND=0V

LOGIC SECTION

Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Unit (Limit)
I_{DDL}	Supply Current	Pins 14, 15, 16 are 0V	0.01	0.5	**0.5**	mA (Max)
I_{SSL}		Pins 14, 15, 16 are 0V	0.01	0.5	**0.5**	mA (Max)
I_{DDH}		Pins 14, 15, 16 are 5V	1.3	5	**5**	mA (Max)
I_{SSH}		Pins 14, 15, 16 are 5V	0.9	5	**5**	mA (Max)
V_{IH}	High-Level Input Voltage	@Pins 14, 15, 16	1.8	2.3	**2.5**	V (Min)
V_{IL}	Low-Level Input Voltage	@Pins 14, 15, 16	0.9	0.6	**0.4**	V (Max)
f_o	Clock Frequency	@Pin 14	2000	500	**500**	kHz (Max)
$t_{w(\overline{STB})}$	Width of $\overline{STB}$ Input	See *Figure 1*	0.25	1	**1**	μs (Min)
t_{setup}	Data Setup Time	See *Figure 1*	0.25	1	**1**	μs (Min)
t_{hold}	Data Hold Time	See *Figure 1*	0.25	1	**1**	μs (Min)
t_{cs}	Delay from Rising Edge of $\overline{CLOCK}$ to $\overline{STB}$	See *Figure 1*	0.25	1	**1**	μs (Min)
I_{IN}	Input Current	@Pins 14, 15, 16 $0V<V_{IN}<5V$	±0.01	±1		μA (Max)
C_{IN}	Input Capacitance	@Pins 14, 15, 16 f=1 MHz	5			pF

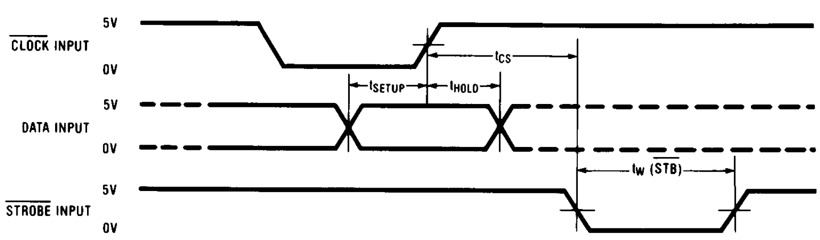
Note 1: Pins 2, 3 and 26 have a maximum input voltage range of ±22V for the typical application shown in *Figure 7*.

Note 2: Bold numbers apply at temperature extremes. All other numbers apply at $T_A=25°C$, $V_{DD}=7.5V$, $V_{SS}=-7.5V$, D.GND=A.GND=0V as shown in the test circuit, *Figures 3* and *4*.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed (but not 100% production tested) over the operating temperature range. These limits are not used to calculate outgoing quality levels.

Timing Diagram



TL/H/6753–3

Note: To change the gain of the presently selected band, it is not necessary to send DATA 1 (Band Selection) each time.

FIGURE 1

Electrical Characteristics (Note 2) $V_{DD}=7.5V$, $V_{SS}=-7.5V$, D.GND = A.GND = 0V

SIGNAL PATH SECTION

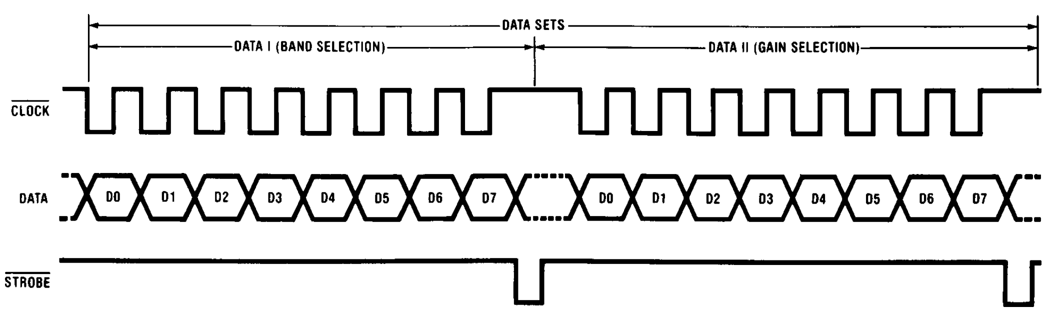
Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Unit (Limit)
E_A	Gain Error	$A_V=0$ dB @ ± 12 dB Range	0.1	0.5	**0.5**	dB (Max)
		$A_V=0$ dB @ ± 6 dB Range	0.1	1	**1**	dB (Max)
		$A_V=\pm1$ dB @ ± dB Range (R_{5b} or R_{5c} is ON)	0.1	0.5	**0.6**	dB (Max)
		$A_V=\pm2$ dB @ ± 12 dB Range (R_{4b} or R_{4c} is ON)	0.1	0.5	**0.6**	dB (Max)
		$A_V=\pm3$ dB @ ± 12 dB Range (R_{3b} or R_{3c} is ON)	0.1	0.5	**0.6**	dB (Max)
		$A_V=\pm4$ dB @ ± 12 dB Range (R_{2b} or R_{2c} is ON)	0.1	0.5	**0.7**	dB (Max)
		$A_V=\pm5$ dB @ ± 12 dB Range (R_{1b} or R_{1c} is ON)	0.1	0.5	**0.7**	dB (Max)
		$A_V=\pm9$ dB @ ± 12 dB Range (R_{0b} or R_{0c} is ON)	0.2	1	**1.3**	dB (Max)
THD	Total Harmonic Distortion	$A_V=0$ dB @ ± 12 dB Range $V_{IN}=4V_{rms}$, f = 1 kHz	0.0015			%
		$A_V=12$ dB @ ± 12 dB Range				
		$V_{IN}=1V_{rms}$, f = 1 kHz	0.01	0.1		% (Max)
		$V_{IN}=1V_{rms}$, f = 20 kHz	0.1	0.5		% (Max)
		$A_V=-12$ dB @ ± 12 dB Range				
		$V_{IN}=4V_{rms}$, f = 1 kHz	0.01	0.1		% (Max)
		$V_{IN}=4V_{rms}$, f = 20 kHz	0.1	0.5		% (Max)
$V_{O\ Max}$	Maximum Output Voltage	$A_V=0$ dB @ ± 12 dB Range THD < 1%, f = 1 kHz	5.5	5.1	**5**	V_{rms} (Min)
S/N	Signal to Noise Ratio	$A_V=0$ dB @ ± 12 dB Range $V_{ref}=1\ V_{rms}$	114			dB
		$A_V=12$ dB @ ± 12 dB Range $V_{ref}=1V_{rms}$	106			dB
		$A_V=-12$ dB @ ± 12 dB Range $V_{ref}=1V_{rms}$	116			dB
I_{LEAK}	Leakage Current	$A_V=0$ dB @ ± 12 dB Range (All internal switches are OFF)				
		Pin 2 + 3, Pin 26		500		nA (Max)
		Pin 5 ~ Pin 11, Pin 18 ~ Pin 24		50		nA (Max)

Note 2; Boldface numbers apply at temperature extremes. All other numbers apply at $T_A=25°C$, $V_{DD}=7.5V$, $V_{SS}=-7.5V$, D.GND = A.GND = 0V as shown in the test circuit, *Figures 3* and *4*.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed (but not 100% production tested) over the operating temperature range. These limits are not used to calculate outgoing quality levels.

Timing Diagrams



TL/H/6753–4

Note: To change the gain of the presently selected band, it is not necessary to send DATA 1 (Band Selection) each time.

FIGURE 2

Truth Tables

DATA I (Band Selection)

(Ch A: Band 1∼7, Ch B: Band 8∼14)

D7	D6	D5	D4	D3	D2	D1	D0	
H	X	L	L	L	L	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, No Band Selection
H	X	L	L	L	L	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 1
H	X	L	L	L	L	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 2
H	X	L	L	L	L	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 3
H	X	L	L	L	H	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 4
H	X	L	L	L	H	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 5
H	X	L	L	L	H	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 6
H	X	L	L	L	H	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 7
H	X	L	L	H	L	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 8
H	X	L	L	H	L	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 9
H	X	L	L	H	L	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 10
H	X	L	L	H	L	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 11
H	X	L	L	H	H	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 12
H	X	L	L	H	H	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 13
H	X	L	L	H	H	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 14
H	X	L	L	H	H	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, No Band Selection
H	X	L	H	Valid Binary Input				Ch A ± 12 dB Range, Ch B ± 6 dB Range, Band 1∼14
H	X	H	L	Valid Binary Input				Ch A ± 6 dB Range, Ch B ± 12 dB Range, Band 1∼14
H	X	H	H	Valid Binary Input				Ch A ± 6 dB Range, Ch B ± 6 dB Range, Band 1∼14
↑ ①	↑ ②	↑ ③	↑ ④	← Band Code →				

① DATA 1
② Don't Care
③ Ch A ±6 dB/±12 dB Range
④ Ch B ±6 dB/±12 dB Range

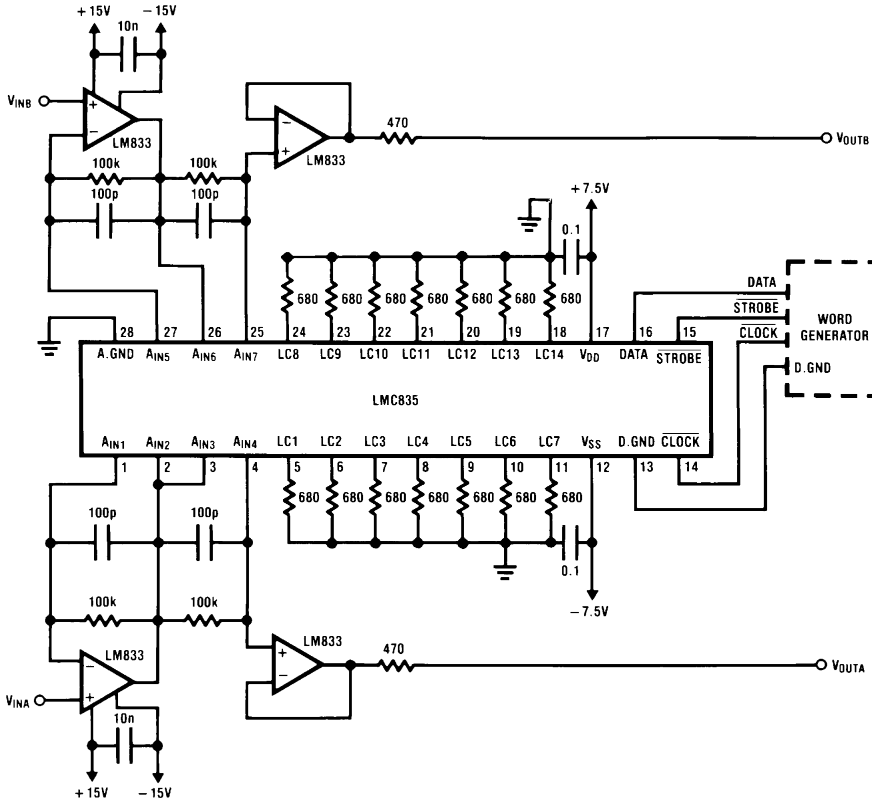
DATA II (Gain Selection)

This is the gain if the ±12 dB range is selected by DATA I. If the ±6 dB range is selected, then the values shown must be approximately halved. See the characteristics curves for more exact data.

	D7	D6	D5	D4	D3	D2	D1	D0
Flat	L	X	L	L	L	L	L	L
1 dB Boost	L	H	H	L	L	L	L	L
2 dB Boost	L	H	L	H	L	L	L	L
3 dB Boost	L	H	L	L	H	L	L	L
4 dB Boost	L	H	L	L	L	H	L	L
5 dB Boost	L	H	L	L	L	L	H	L
6 dB Boost	L	H	L	H	L	L	H	L
7 dB Boost	L	H	H	L	H	L	H	L
8 dB Boost	L	H	L	H	L	H	H	L
9 dB Boost	L	H	L	L	L	L	L	H
10 dB Boost	L	H	H	L	H	L	L	H
11 dB Boost	L	H	H	L	H	H	L	H
12 dB Boost	L	H	H	L	H	H	H	H
1 dB∼12 dB Cut	L	L	Valid Above Input					
	↑ ⑤	↑ ⑥	← Gain Code →					

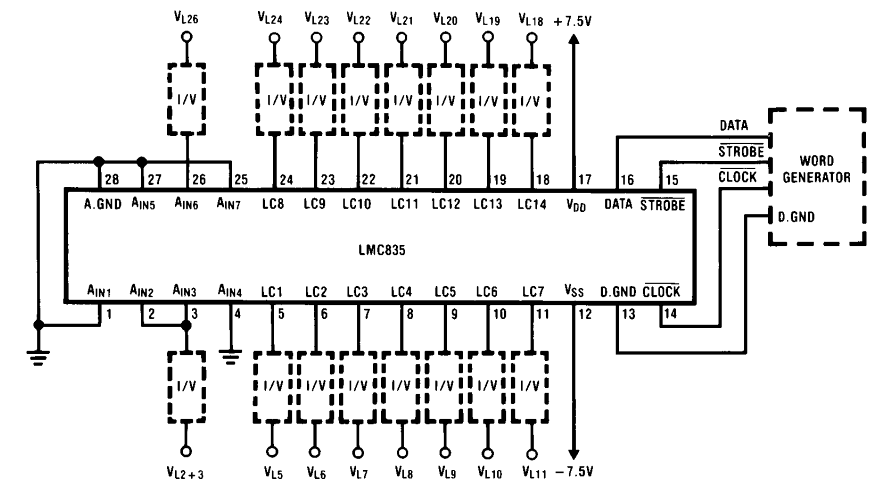
⑤ DATA II
⑥ Boost/Cut

Test Circuits



TL/H/6753–5

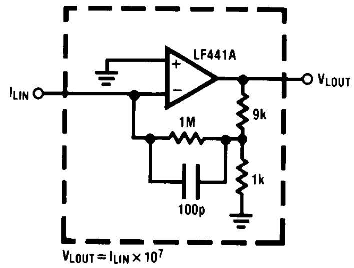
FIGURE 3. Test Circuit for AC Measurement



TL/H/6753–6

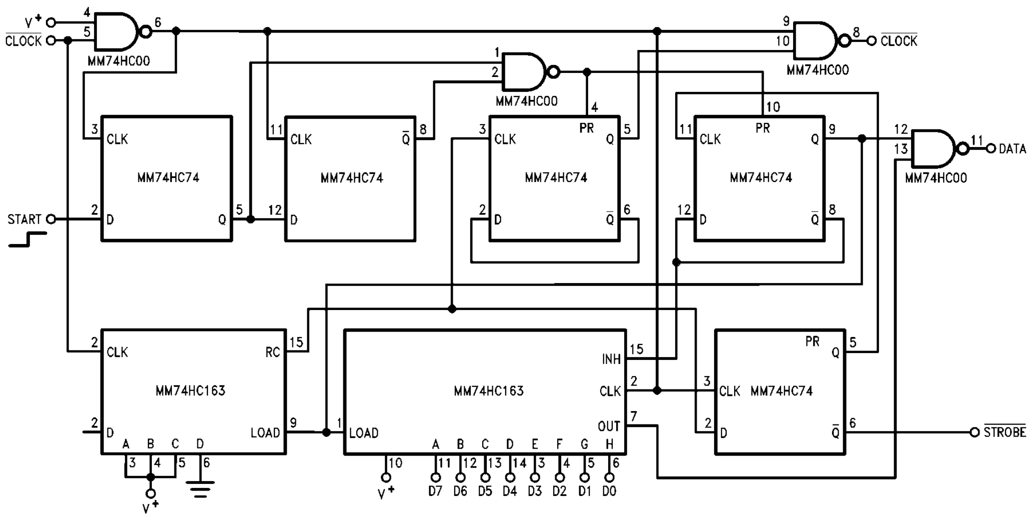
FIGURE 4. Test Circuit for Leakage Current Measurement

Test Circuits (Continued)



TL/H/6753–7

FIGURE 5. I to V Converter

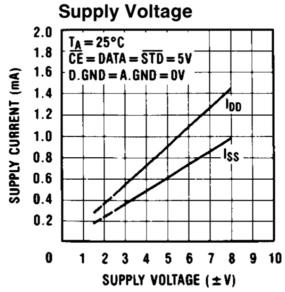


TL/H/6753–8

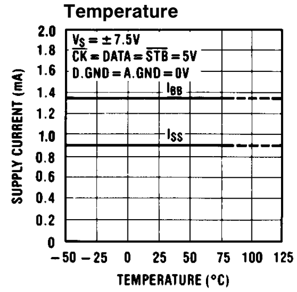
FIGURE 6. Simple Word Generator

Typical Performance Characteristics

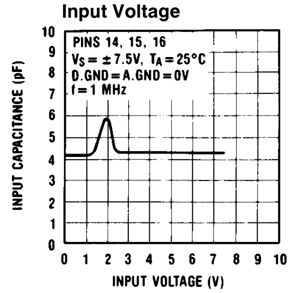
Supply Current vs Supply Voltage



Supply Current vs Temperature



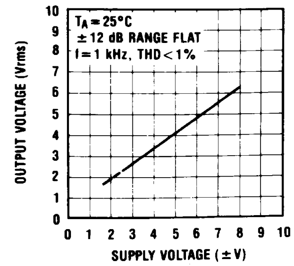
Input Capacitance vs Input Voltage



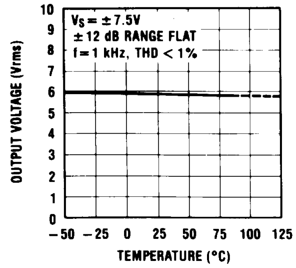
TL/H/6753–9

Typical Performance Characteristics (Continued)

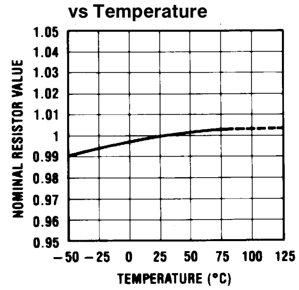
Maximum Output Voltage vs Supply Voltage



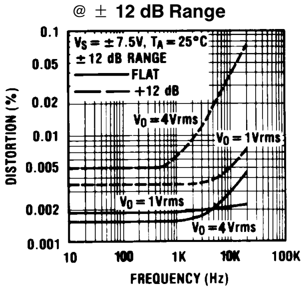
Maximum Output Voltage vs Temperature



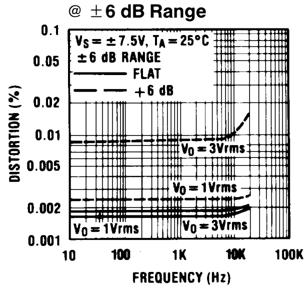
Nominal Resistor vs Temperature



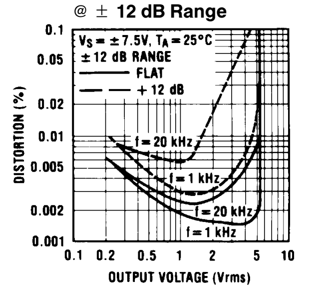
Distortion vs Frequency @ ± 12 dB Range



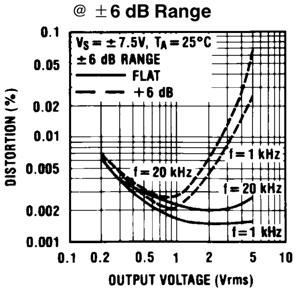
Distortion vs Frequency @ ±6 dB Range



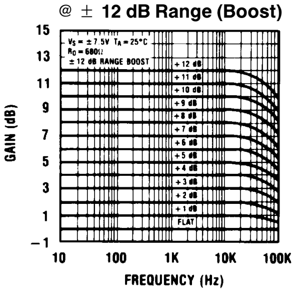
Distortion vs Output Voltage @ ± 12 dB Range



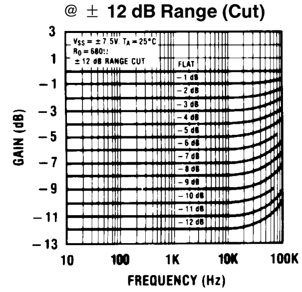
Distortion vs Output Voltage @ ±6 dB Range



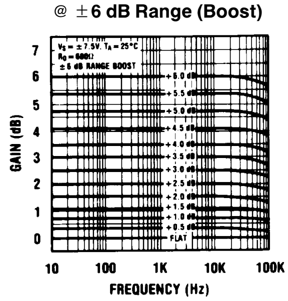
Gain vs Frequency @ ± 12 dB Range (Boost)



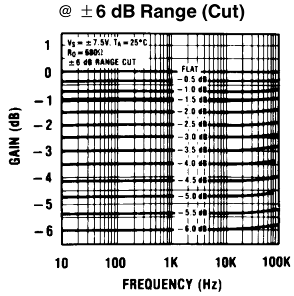
Gain vs Frequency @ ± 12 dB Range (Cut)



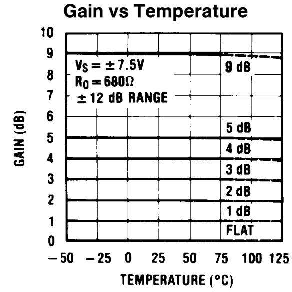
Gain vs Frequency @ ±6 dB Range (Boost)



Gain vs Frequency @ ±6 dB Range (Cut)

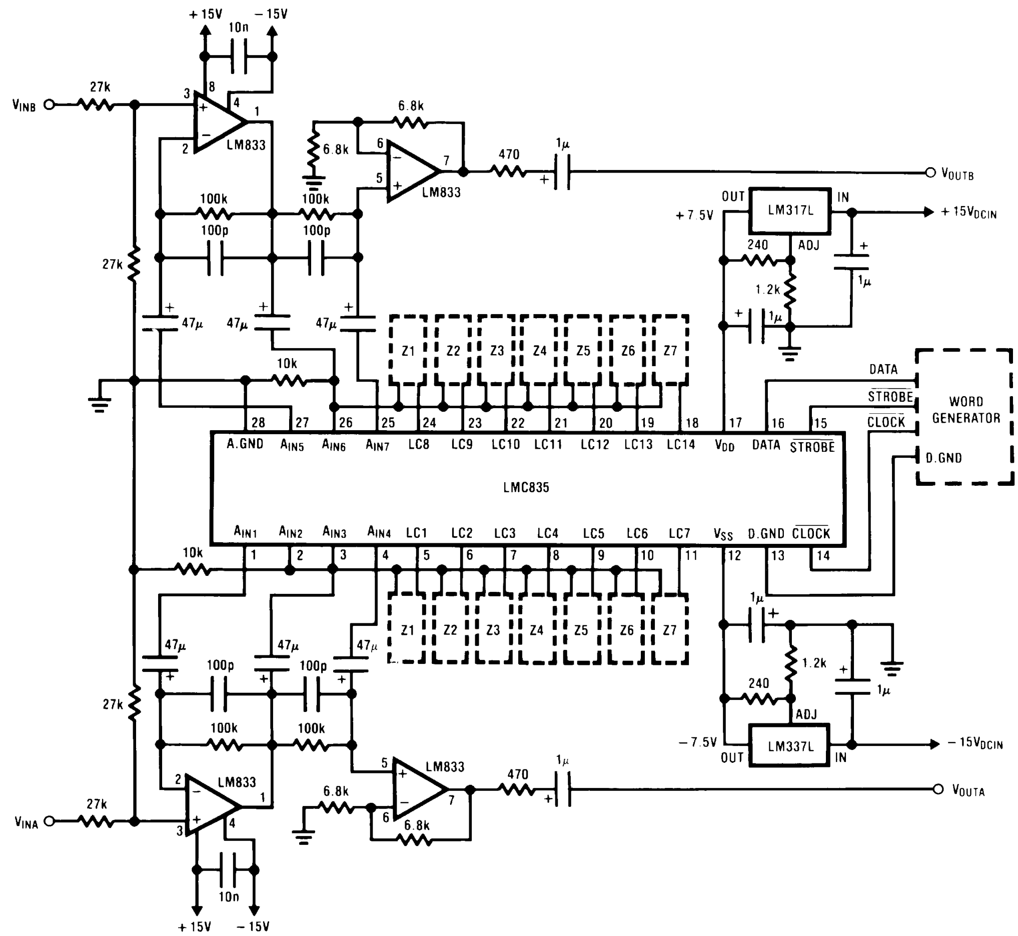


Gain vs Temperature



TL/H/6753–10

Typical Applications

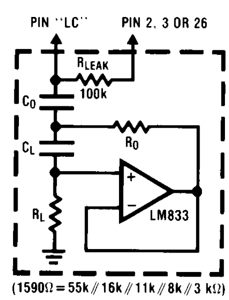


TL/H/6753–11

FIGURE 7. Stereo 7-Band Equalizer

TABLE I: Tuned Circuit Elements

$Q_0 = 3.5$, $Q_{12dB} = 1.05$					
Z1	**f_O (Hz)**	**C_O (F)**	**C_L (F)**	**R_L (Ω)**	**R_O (Ω)**
Z1	63	1µ	0.1µ	100k	680
Z2	160	0.47µ	0.033µ	100k	680
Z3	400	0.15µ	0.015µ	100k	680
Z4	1k	0.068µ	0.0068µ	82k	680
Z5	2.5k	0.022µ	0.0033µ	82k	680
Z6	6.3k	0.01µ	0.0015µ	62k	680
Z7	16k	0.0047µ	680p	47k	680



$L_O = C_L R_L R_O$

$f_O = \frac{1}{2\pi\sqrt{L_O C_O}}$

$Q_O = \sqrt{\frac{L_O}{C_O R_O^2}}$

$Q_{12\,dB} = \frac{R_O Q_O}{R_O + 1590}$

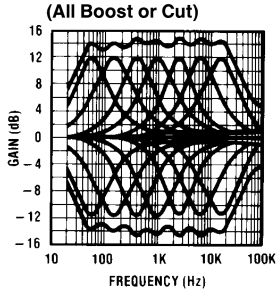
TL/H/6753–12

FIGURE 8. Tuned Circuit for Stereo 7-Band Equalizer (*Figure 7*)

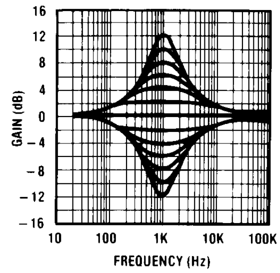
Typical Applications (Continued)

Performance Characteristics (Circuit of *Figure 7*)

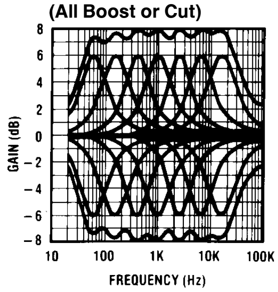
LMC835 Gain vs Frequency @ ± 12 dB Range (All Boost or Cut)



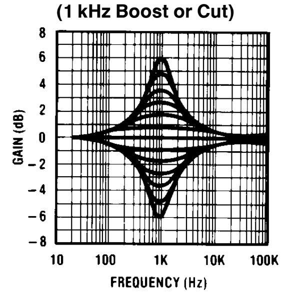
LMC835 Gain vs Frequency @ ± 12 dB Range (1 kHz Boost or Cut)



LMC835 Gain vs Frequency @ ±6 dB Range (All Boost or Cut)



LMC835 Gain vs Frequency @ ±6 dB Range (1 kHz Boost or Cut)



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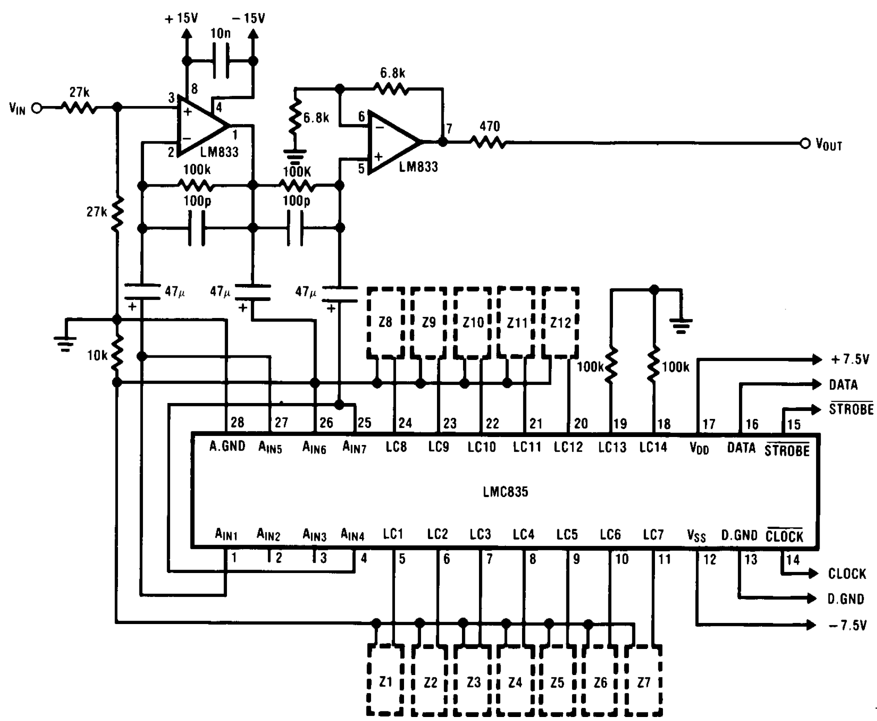

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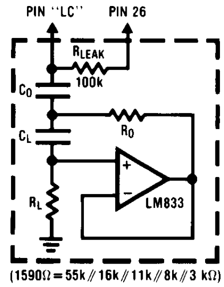
FIGURE 9. 12-Band Equalizer

Typical Applications (Continued)

TABLE II. Tuned Circuit Elements

$Q_0 = 4.7$, $Q_{12\,dB} = 1.4$					
	f_o (Hz)	C_o (F)	C_L (F)	R_L (Ω)	R_o (Ω)
Z1	16	3.3μ	0.47μ	100k	680
Z2	31.5	15μ	0.22μ	110k	680
Z3	63	1μ	0.1μ	100k	680
Z4	125	0.39μ	0.068μ	91k	680
Z5	250	0.22μ	0.033μ	82k	680
Z6	500	0.1μ	0.015μ	100k	680
Z7	1k	0.047μ	0.01μ	82k	680
Z8	2k	0.022μ	0.0047μ	91k	680
Z9	4k	0.01μ	0.0022μ	110k	680
Z10	8k	0.0068μ	0.001μ	82k	680
Z11	16k	0.0033μ	680p	62k	680
Z12	32k	0.0015μ	470p	68k	510



$L_0 = C_L R_L R_0$

$f_0 = \frac{1}{2\pi\sqrt{L_0 C_0}}$

$Q_0 = \sqrt{\frac{L_0}{C_0 R_0^2}}$

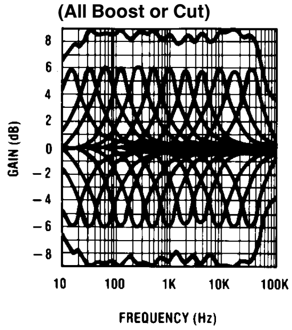
$Q_{12\,dB} = \frac{R_0 Q_0}{R_0 + 1590}$

TL/H/6753–15

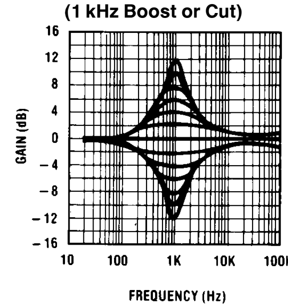
FIGURE 10. Tuned Circuit for 12-Band Equalizer (*Figure 9*)

Performance Characteristics (Circuit of Figure 9)

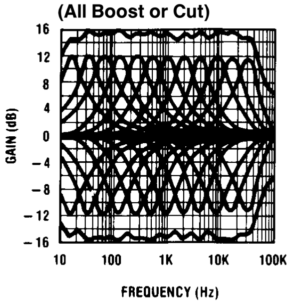
12 Band Equalizer Application LMC835 Gain vs Frequency @ ±6 dB Range (All Boost or Cut)



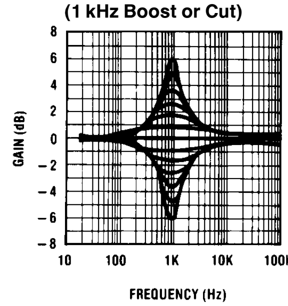
LMC835 12 Band E.Q. Application Gain vs Frequency @ ±12 dB Range (1 kHz Boost or Cut)



12 Band Equalizer Application LMC835 Gain vs Frequency @ ± 12 dB Range (All Boost or Cut)

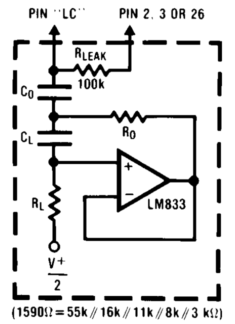


LMC835 12 Band E.Q. Application Gain vs Frequency @ ±6dB Range (1 kHz Boost or Cut)



TL/H/6753–16

Typical Applications (Continued)



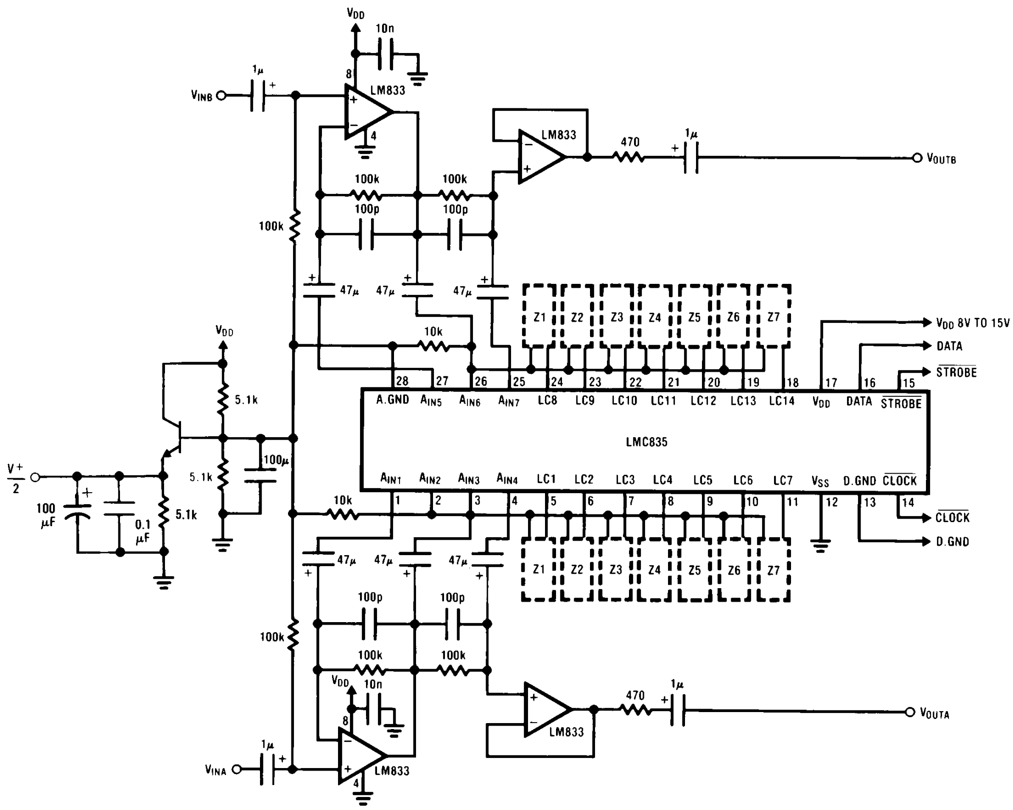
$L_o = C_L, R_L, R_O$

$F_o = \frac{1}{2\pi\sqrt{L_O C_O}}$

$Q_O = \sqrt{C_O R_O^2}$

$Q_{12\,dB} = \frac{R_O Q_O}{R_O + 15°C}$

TL/H/6753–25

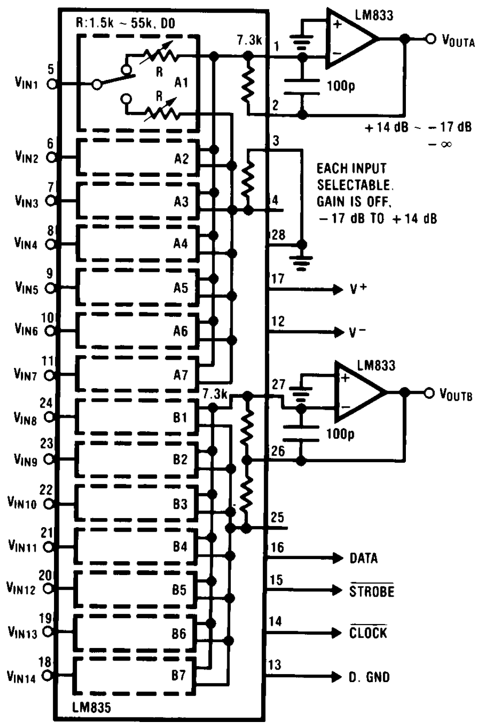


TL/H/6753–17

The $\frac{V^+}{2}$ output is used to bias the gyrators

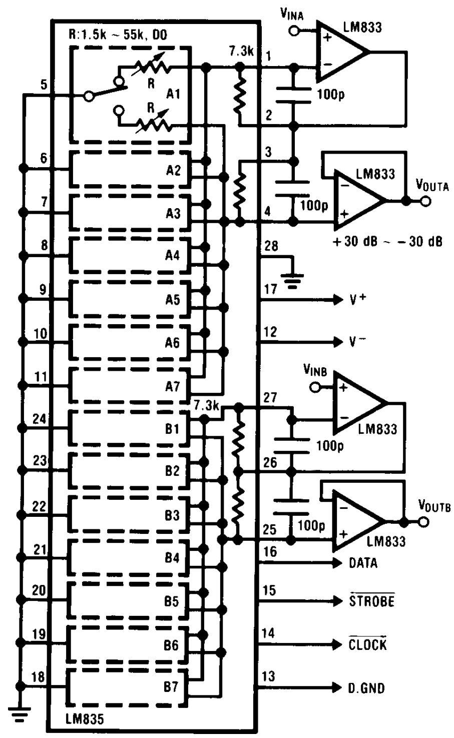
FIGURE 11. Single Supply Stereo Equalizer

Typical Applications (Continued)



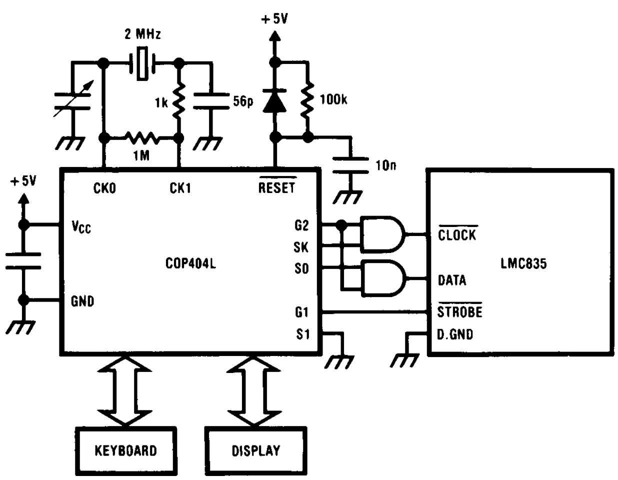
TL/H/6753–18

FIGURE 12. Stereo 7-Input/1-Output Mixers (THD is not as low as equalizer circuit)



TL/H/6753–19

FIGURE 13. Stereo Volume Control, Very Low THD



TL/H/6753–20

FIGURE 14. LMC835-COP404L CPU Interface

Typical Applications (Continued)

Sample Subroutine Program for *Figure 14*, LMC835-COP404L CPU Interface

```
HEX
CODE    LABEL      MNEMONICS         COMMENTS
3F      LMC835:    LBI     3F        ;POINT TO RAMADDRESS 3F
05      SEND       LD                ;RAMDATA TO A
22                 SC                ; SET CARRY
335F               OGI               ;SET PORT G= 1111, OPEN THE AND GATES
4F                 XAS               ;SWAP A AND SIO, CLOCK START
05                 LD                ;RAMDATA TO A, MAKE SURE A = DATA
07                 XDS               ;SWAP A AND RAMDATA, RAMADDRESS=RAMADDRESS-1
05                 LD                ;RAMDATA TO A
4F                 XAS               ;SWAP A AND SIO
05                 LD                ;RAMDATA TO A, MAKE SURE A=NEWDATA
07                 XDS               ;SWAP A AND RAMDATA, RAMADDRESS=RAMADDRESS-1
32                 RC                ;RESET CARRY
4F                 XAS               ;SWAP A AND SIO, CLOCK STOP
335D               OGJ     13        ;SET PORT G=1101, MAKE STROBE LOW
335B               OGI     11        ;SET PORT G=1011, MAKE STROBE HIGH, CLOSE THE
                                                            GATES
4E                 CBA               ;BD TO A
43                 AISC    3         ;RAMADDRESS<3C THEN RETURN
48                 RET
80                 JP      SEND
```

```
   RAM
 ADDRESS          COMMENTS
3C      DATA      ;GAIN DATA D4-D7
3D      DATA      ;GAIN DATA D0-D3
3E      DATA      ;BAND DATA D4-D7
3F      DATA      ;BAND DATA D0-D3
```

Application Hints

SWITCHING NOISE

The LMC835 uses CMOS analog switches that have small leakages (less than 50 nA). When a band is selected for flat gain, all the switches in that band are open and the resonator circuit is not connected to the LMC835 resistor network. It is only in the flat mode that the small leakage currents can cause problems. The input to the resonator circuit is usually a capacitor and the leakage currents will slowly charge up this capacitor to a large voltage if there is no resistive path to limit it. When the band is set to any value other than flat, the charge on the capacitor will be discharged by the resistor network and there will be a transient at the output. To limit the size of this transient, R_{LEAK} is necessary.

HOW TO AVOID SWITCHING NOISE DUE TO LEAKAGE CURRENT (Refer to *Figures 7* and *8*)

To avoid switching noise due to leakage currents when changing the gain, it is recommended to put $R_{LEAK} = 100$ kΩ between Pin 3 and Pin 5—11 each, Pin 26 and Pin 12—24 each. The resistor limits the voltage that the capacitor can charge to, with minimal effects on the equalization. The frequency response change due to R_{LEAK} are shown in *Figure 15*. The gain error is only 0.2 dB and Q error is only 5% at 12 dB boost or cut.

SIMPLE WORD GENERATOR *(Figure 6)*

Circuit operation revolves around an MM74HC165 parallel-in/serial-out shift register. Data bits D0 through D7 are applied to the parallel of the MM74HC165 from 8 toggle switches. The bits are shifted out to the DATA input of the LMC835 in sync with the clock. When all data bits have been loaded, CLOCK is inhibited and a STROBE pulse is generated: this sequence is initiated by a START pulse.

LMC835-COP404L CPU INTERFACE (Refer to *Figure 14*)

The diagram shows AND gates between the COP and the LMC835. These permit G2 to inhibit the CLOCK and DATA lines (SK and SO) during a STROBE (G1) pulse. This function may also be implemented in software. As shown in *Figure 2*, the data groups are shifted in D0 first. Data is loaded on positive clock edges.

POWER SUPPLIES

These applications show LM317/337 regulators for the $\pm$7.5V supplies for the LMC835. Since the latter draws only 5 mA max., 1k series dropping resistors from the $\pm$15V op amp supply and a pair of 7.5V zeners and bypass caps will also suffice.

Application Hints (Continued)

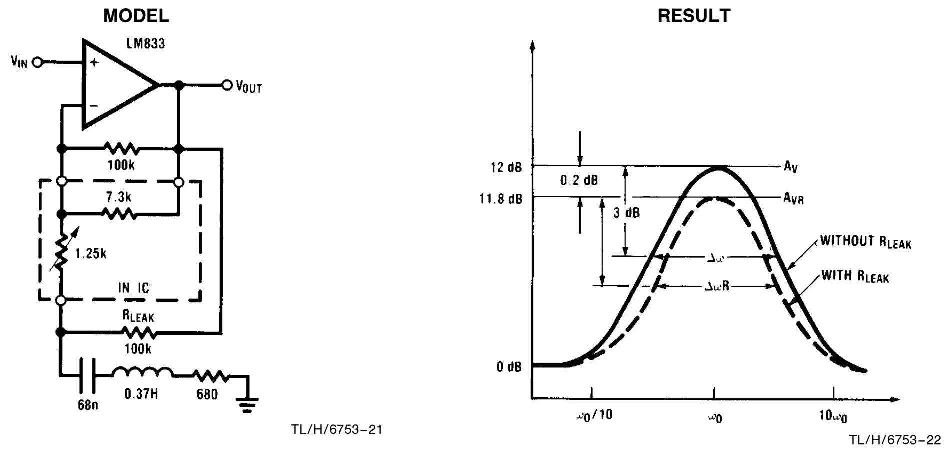


FIGURE 15. Effect of R_{LEAK}

REDUCING EXTERNAL COMPONENTS

The typical application shown in *Figure 7* is switching noise free. The DC-coupled circuit in *Figure 16* is also switching noise free, except at 12 dB/6 dB switch turn ON/OFF. This switching noise is caused by the I_{bias} and V_{offset} of the op amps. Selecting a low I_{bias} and V_{offset} op amp can minimize the switching noise due to the 12 dB/6 dB switch. The DC-coupled application can also eliminate the $R_F = 100k$ resistors with only a 0.5 dB gain error at 12 dB boost or cut.

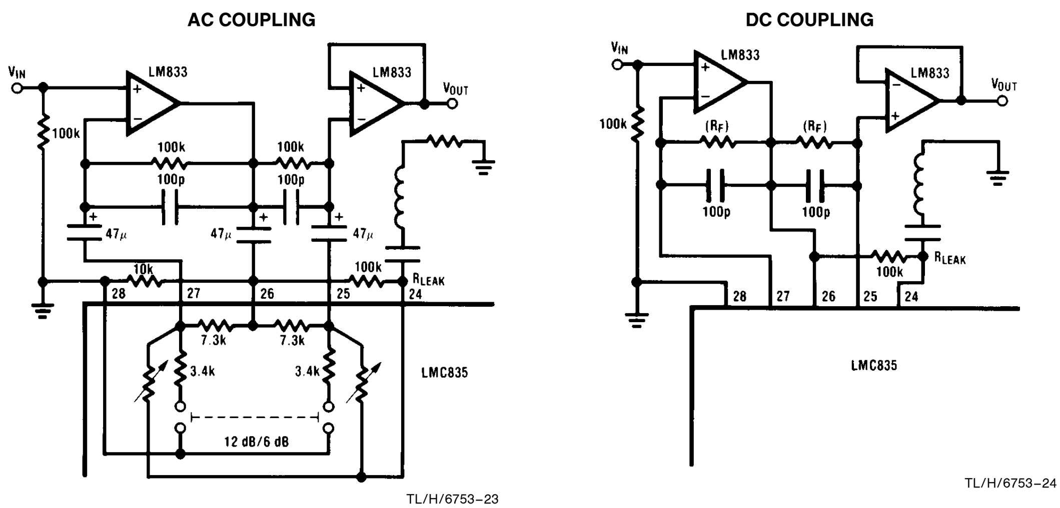
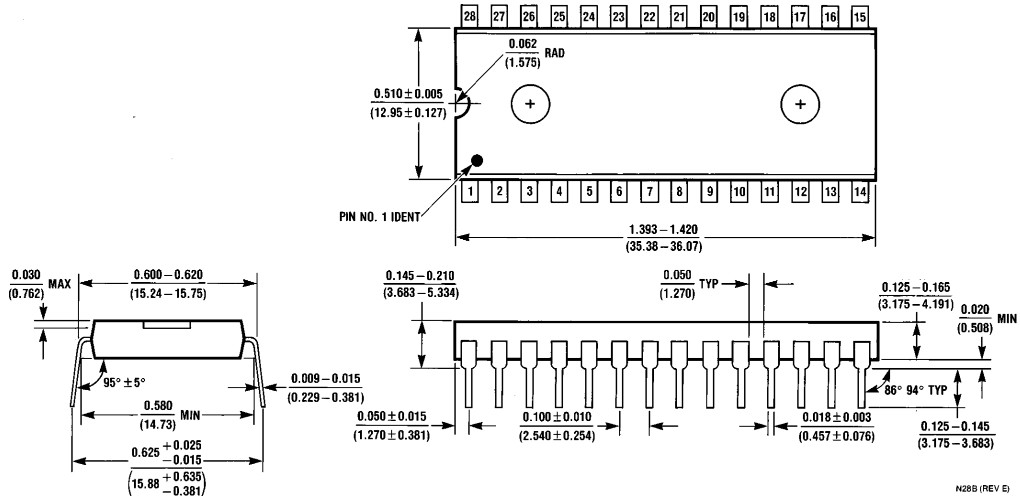


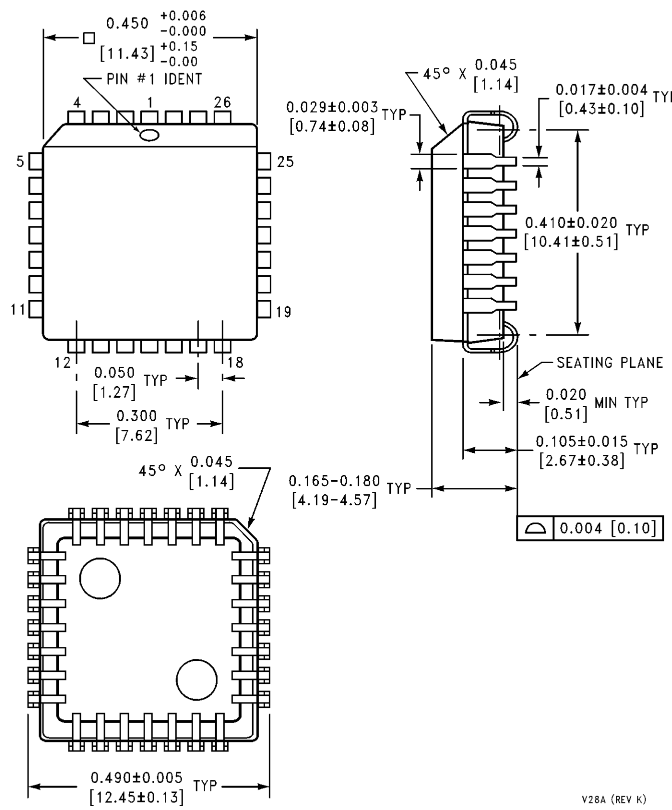
FIGURE 16. Reducing External Components

Physical Dimensions inches (millimeters)



Order Number LMC835N
NS Package N28B

Physical Dimensions inches (millimeters) (Continued)



Order Number LMC835V
NS Package V28A

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