MOTOROLA

SEMICONDUCTORS

3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MC145433
MC145434

Advance Information

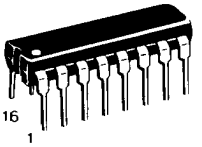
CMOS
(LOW-POWER COMPLEMENTARY MOS)

TUNEABLE NOTCH/ BAND-PASS FILTERS

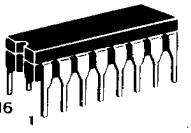
NOTCH/BAND-PASS FILTERS

These devices contain a 6-pole notch filter and 4-pole band-pass filter. The MC145433 has the option of both filters being independently tuned with one or two external clocks. The MC145434 requires both filters to be tuned together with one external clock.

- ±5 to ±8 V Supply Operation
- Low Power Consumption, 80 mW Typical
- Independently Tuneable Notch and Band-pass Filters
- On-board Crystal Oscillator or External Clocks
- Clock Output Pin
- An Uncommitted Op-Amp Is Provided Capable of Driving 600 Ω Loads
- Notch Filter Output Gain Adjustable
- TTL or CMOS Compatible Digital Inputs
- 16-Pin Package

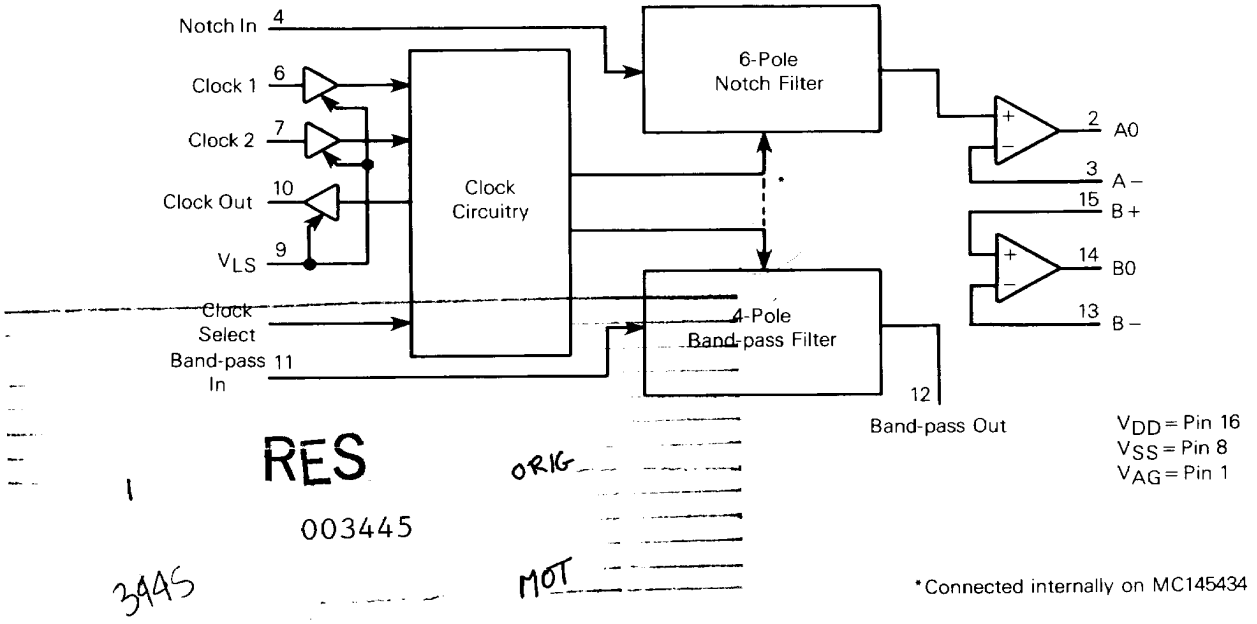


P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

BLOCK DIAGRAM



*Connected internally on MC145434

RES
ORIG
003445
3945
MOT

MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD}+0.5	V
DC Current Drain Per Pin (Not V_{DD} or V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	10	15	16	V

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V, T_A = 25°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Operating Current, V_{DD} = 12 V		I_{DD}	–	4.5	TBD	mA
Input Capacitance		C_{in}	–	5.0	7.5	pF
MODE CONTROL LOGIC LEVELS						
V_{LS} TTL Mode		–	V_{SS}	–	V_{DD}−4	V
V_{LS} CMOS Mode		V_{IH}	V_{DD}−0.5	–	V_{DD}	V
Clock Select	State 1	V_{IH}	V_{DD}−0.5	–	V_{DD}	V
Clock Select	State 2	V_{IM}	V_{SS}+4	–	V_{DD}−4	V
Clock Select	State 3	V_{IL}	V_{SS}	–	V_{SS}+0.5	V
C1, C2	**TTL LOGIC LEVELS (V_{LS} = 5 V, V_{SS} = 0 V)**					
Input Current	"1" Level	I_{IH}	–	–	±0.03	μA
Input Current	"0" Level	I_{IL}	–	–	±0.03	μA
Input Voltage	"1" Level	V_{IH}	V_{LS}+2.0	–	–	V
Input Voltage	"0" Level	V_{IL}	–	–	V_{LS}+0.8	V
C1, C2	**CMOS LOGIC LEVELS (V_{LS} = V_{DD}, V_{SS} = 0 V)**					
Input Current	"1" Level	I_{IH}	–	–	±0.03	μA
Input Current	"0" Level	I_{IL}	–	–	±0.03	μA
Input Voltage	"1" Level V_{DD} = 12 V V_{DD} = 15 V	V_{IH}	9.0 11.5	6.75 8.25	– –	V
Input Voltage	"0" Level V_{DD} = 12 V	V_{IL}	– –	5.25 6.75	3.6 4.0	V

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 15 V, V_{AG} = 7.5 V, V_{SS} = 0 V, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Input Current, V_{AG}	I_I	–	–	±10	μA
DC Input Current, NI and BPI	I_I	–	–	±1.0	μA
AC Input Impedance (1 kHz) NI and BPI	Z_{in}	0.2	1.0	–	M
Input Voltage Range, NI and BPI	V_{in}	V_{SS}+1.5	–	V_{DD}−1.5	V

OP-AMP CHARACTERISTICS (V_{DD} = 12 to 15 V, $V_{AG} = V_{DD}/2$, T_A = 0 to 70°C)

Characteristic	Symbol	Type	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	A	–	–	±50	mV
		B	–	–	±50	
Open Loop Gain (R_L = 10 kΩ)	A_{OL}	A	–	45	–	dB
		B	–	60	–	
Input Bias Current	I_{IB}	A,B	–	±0.1	–	μA
Output Noise (900 Ω)	P_N	A	–	−3	0	dBrnc
Slew Rate	S_R	A	–	2	–	V/μS
Output Voltage Swing R_L = 20 kΩ to V_{AG}	V_O	A	1.5	–	$V_{DD}-1.5$	V
		B	1.5	–	$V_{DD}-1.5$	
R_L = 900 Ω to V_{AG}		A	1.5	–	$V_{DD}-1.5$	V
		B	$V_{AG}-2.0$	–	$V_{AG}+2.0$	
R_L = 600 Ω to V_{AG}		A	$V_{AG}-4.0$	–	$V_{AG}+4.0$	V
		B	$V_{AG}-1.4$	–	$V_{AG}+1.4$	

Type refers to the op amp type described in the pin descriptions.

DIGITAL SWITCHING CHARACTERISTICS (V_{DD} = 15 V, V_{SS} = 0, T_A = 25°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Rise and Fall Times	C1, C2	t_r, t_f	–	–	4	μs
Input Pulse Width (TTL Mode)	C1, C2	t_w	200	–	–	ns
Clock Frequency (TTL Mode)	C1, C2	f_c	–	–	2.048	MHz
Clock Frequency (CMOS Mode)	C1, C2	f_c	–	–	4	MHz
Crystal Frequency	C1, C2	f_x	1	–	4	MHz
Input Pulse Width (CMOS Mode)	C1, C2	t_w	125	–	–	ns
Switching Frequency (Internal)		f_s	10	–	400	kHz

CO OUTPUT CHARACTERISTICS (V_{DD} = 12 V to 15 V, V_{SS} = 0 V, T_A = 25°C)

Characteristic		Symbol	Min	Typ	Max	Unit
TTL Output Voltage	I_O = 100 μA, "1"	V_{OH}	2.4	–	–	V
TTL Output Voltage	I_O = 0.8 mA, "0"	V_{OL}	–	–	0.4	V
CMOS Output Current	V_{DD} = 12 V, V_{OH} = 9.3 V	I_{OH}	−1.1	−2.25	–	mA
	V_{DD} = 15 V, V_{OH} = 13.5 V	I_{OH}	−3.0	−8.8	–	mA
CMOS Output Current	V_{DD} = 12 V, V_{OL} = 0.5 V	I_{OL}	1.1	2.25	–	mA
	V_{DD} = 15 V, V_{OL} = 1.5 V	I_{OL}	3.0	8.8	–	mA

FIGURE 2 — TYPICAL NOTCH FILTER RESPONSE CURVES

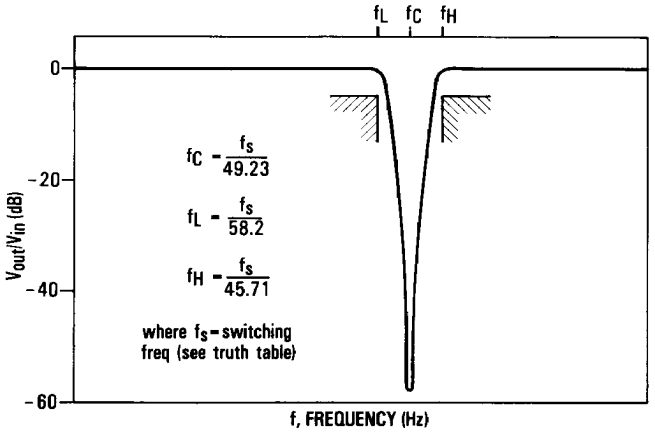
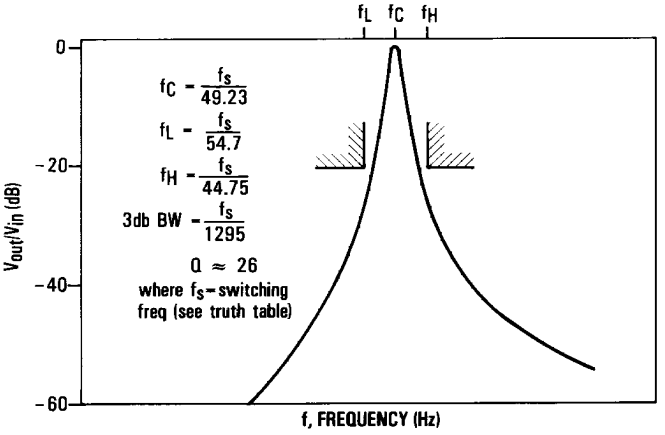


FIGURE 3 — TYPICAL BAND-PASS FILTER RESPONSE CURVES



NOTCH FILTER ELECTRICAL CHARACTERISTICS (V_{DD} = 15 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 25°C)

Characteristic*		Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dbm0)		V_{FS}	12	–	–	V_{PP}
Gain at 385 Hz		A_r	−0.5	0.0	0.5	dB
Idle Noise, NI = V_{AG}, 900 Ω		P_N	–	–	25	dBrnc
Dynamic Range (V_{FS}/Idle Noise)		DR	80	–	–	dB
Total Harmonic Distortion (0 dbm0)		THD	–	–	1.0	%
Power Supply Rejection Ratio (dc)		PSSR	40	–	–	dB
Output Offset		VOS	−250	–	250	mV
Pass-band Ripple (Ref 385 Hz)	77 - 846 Hz	–	−0.5	–	+0.5	dB
	1.3 kHz - 1.54 kHz		−0.5	–	+0.5	
Rejection	846 - 923 Hz	–	+1.0	–	−5.0	dB
	1.08 kHz - 1.15 kHz		+1.0	–	−5.0	
	1.15 kHz - 1.3 kHz		+1.0	–	−1.0	
	992 - 996 Hz		−45	–	–	
	1003 - 1007 Hz		−45	–	–	
	996 - 1003 Hz		−50	–	–	

*f_S = 49.23 kHz

BAND-PASS FILTER ELECTRICAL CHARACTERISTICS (V_{DD} = 15 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 25°C)

Characteristic*		Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dbm0)		V_{FS}	12	–	–	V_{PP}
Gain at 1000 Hz		A_r	−0.8	0.0	+0.8	dB
Idle Noise, BPI = V_{AG}, 900 Ω		P_N	–	–	33	dBrnc
Dynamic Range (V_{FS}/Idle Noise)		DR	70	–	–	dB
Total Harmonic Distortion (0 dbm0)		THD	–	–	1.0	%
Power Supply Rejection Ratio (dc)		PSSR	40	–	–	dB
Output Offset		VOS	−250	–	250	mV
Rejection (Ref 1000 Hz)	980 Hz	–	−3	–	–	dB
	1018 Hz		−3	–	–	
	900 Hz		−20	–	–	
	1100 Hz		−20	–	–	

*f_S = 49.23 kHz

PIN DESCRIPTIONS

V_{DD} – Most positive supply, nominally +12 V to +15 V.

V_{SS} – Most negative supply, nominally 0 V.

V_{AG} – Analog ground. This pin is a high impedance input which serves as analog ground reference. This pin is nominally held at (V_{DD}-V_{SS})/2.

Clk Sel, Clock Select – This pin control the configuration of the digital section of the circuit. Three different configurations can be obtained by tying this pin to either V_{DD}, V_{AG} or V_{SS}.

V_{LS}, Logic Shift Voltage – This determines the logic levels expected at the digital input pins C1 and C2. If tied to V_{DD}, CMOS logic levels are expected; if tied to a voltage less than V_{DD} − 4 V, TTL levels are expected with V_{LS} equal to logic ground. This pin also controls the output swing at pin C0 in a similar manner, i.e., TTL or CMOS levels.

C1, C2, Clock 1, Clock 2 – When Clk Sel is tied to V_{DD}, a 1 to 4 MHz crystal is tied to C1 and C2. The switching frequency, f_S, of both filters is determined by the crystal frequency and is given by:

$$\frac{\text{f crystal}}{28} = f_S$$

MC145433 – When Clk Sel is tied to V_{AG}, C1 controls the switching frequency f_S for the notch filter, Filter 1, while C2 controls the switching frequency f_S for the band-pass filter, Filter 2. The external clock signals present at C1 and C2 are divided by 16 to arrive at the switching frequency for the filters.

MC145434 — When Clk Sel is tied to V_{AG}, C2 controls the switching frequency f_S for the notch filter, Filter 1, and the bandpass filter, Filter 2. The external clock signal present at C2 is divided by 16 to arrive at the switching frequency for the filters. C1 should be tied to logic ground.

When Clk Sel is tied to V_{SS}, operation is identical to that when tied to V_{AG}, except that the clocks are divided by 1 instead of 16.

Both filters are tuneable with their switching frequency.

NI, A0, A−, Notch In, Op-amp Out, Op-amp Input — Pin NI is the input to the notch filter, Filter 1. The output of this filter is tied to the noninverting input of a Type A op-amp, whose output is pin A0 and inverting input is Pin A−.

MC145433—CO, Clock Out — This pin is the clock output pin. It is equal to the switching frequency, f_S, of the notch filter.

MC145434—CO, Clock Out — This pin is a clock output pin which is selectable with pin 5. With Clk Sel tied to V_{DD}, this crystal frequency is divided by 1376, and is output at this pin. When Clk Sel is held at V_{AG}, the externally applied clock frequency at C1 is divided by 788 and is output at this pin. When Clk Sel is at V_{SS}, the externally applied clock is output at this pin.

BPI, Band-pass In — This is the input to the band-pass filter, Filter 2.

BPO, Band-pass Out — This is the output of the band-pass filter, Filter 2, and is driven by a Type B op-amp output.

B+ — This pin is the noninverting input to the uncommitted Type A of op-amp provided on the circuit.

B− — This pin is the inverting input to the uncommitted Type A op-amp provided on the circuit.

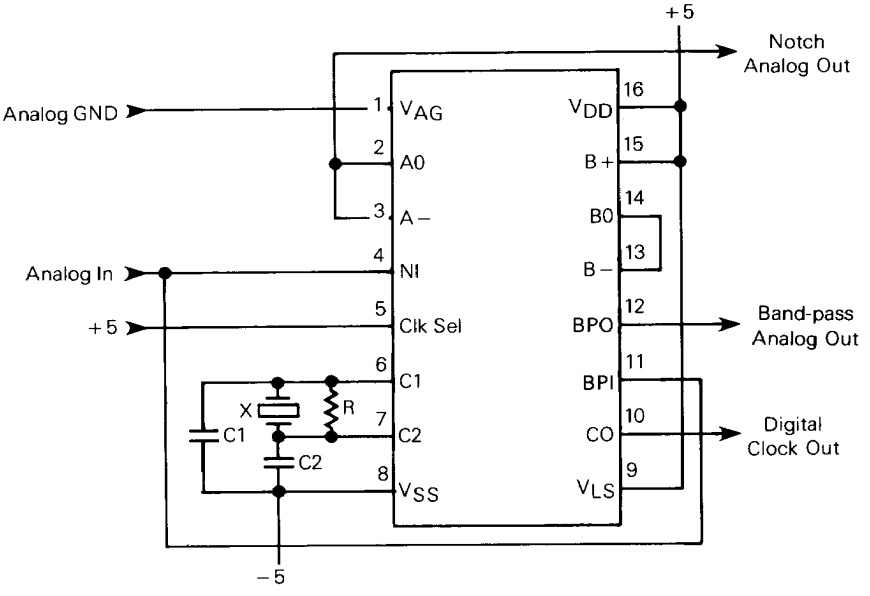
B0 — This pin is the output of the uncommitted Type A op-amp provided on the circuit.

FUNCTIONAL TRUTH TABLE

CLK Sel Pin	Clock Source	Filter Switching Frequency f_S	Notch/Bandpass Center Frequency f_C	Digital Clock Out CO	
				MC145433	MC145434
	Crystal	$f_S = \frac{\text{CLOCK (Hz)}}{28}$	$f_C = \frac{\text{CLOCK (Hz)}}{1378.44}$	$CO = f_S$	$CO = \frac{\text{Crystal}}{1376}$
V_{AG}	External	$f_S = \frac{\text{CLOCK (Hz)}}{16}$	$f_C = \frac{\text{CLOCK (Hz)}}{787.69}$	$CO = f_S$ of Notch	$CO = \frac{\text{EXT CLOCK}}{788}$
V_{SS}	External	f_S = CLOCK (Hz)	$f_C = \frac{\text{CLOCK (Hz)}}{49.23}$	$CO = f_S$ of Notch	$CO = f_S$

NOTE: Switching Frequency (f_S) Range = 10 kHz to 400 kHz

FIGURE 1 — TEST CIRCUIT



R = 10 MΩ
C1, C2 = 30 pF