



# OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS; OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

The SN54/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state.

The SN54/74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN54/74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

## PIN NAMES

D <sub>0</sub> -D <sub>7</sub>	Data Inputs
LE	Latch Enable (Active HIGH) Input
CP	Clock (Active HIGH going edge) Input
OE	Output Enable (Active LOW) Input
O <sub>0</sub> -O <sub>7</sub>	Outputs (Note b)

## LOADING (Note a)

	HIGH	LOW
D <sub>0</sub> -D <sub>7</sub>	0.5 U.L.	0.25 U.L.
LE	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
OE	0.5 U.L.	0.25 U.L.
O <sub>0</sub> -O <sub>7</sub>	65 (25) U.L.	15 (7.5) U.L.

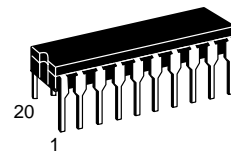
## NOTES:

- a) 1 TTL Units Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.  
 b) The Output LOW drive factor is 7.5 U.L. for Military (54) and 25 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

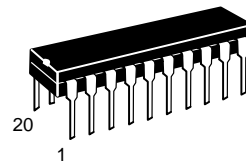
**SN54/74LS373**  
**SN54/74LS374**

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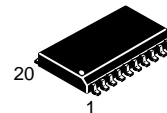
**LOW POWER SCHOTTKY**



**J SUFFIX  
CERAMIC  
CASE 732-03**



**N SUFFIX  
PLASTIC  
CASE 738-03**



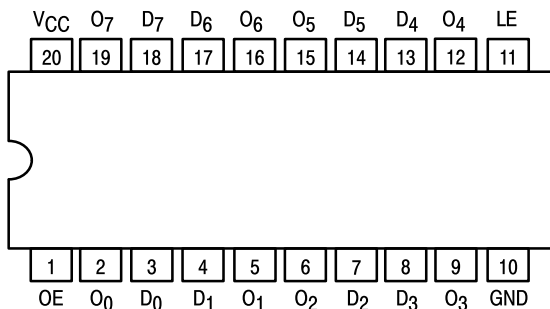
**DW SUFFIX  
SOIC  
CASE 751D-03**

## ORDERING INFORMATION

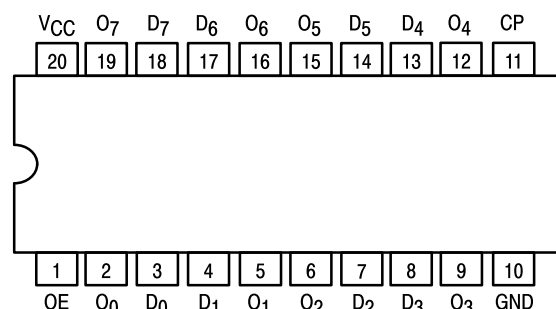
SN54LSXXXJ Ceramic  
 SN74LSXXXN Plastic  
 SN74LSXXXDW SOIC

## CONNECTION DIAGRAM DIP (TOP VIEW)

### SN54/74LS373



### SN54/74LS374



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

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## TRUTH TABLE

LS373

D <sub>n</sub>	LE	OE	O <sub>n</sub>
H	H	L	H
L	H	L	L
X	L	L	Q <sub>0</sub>
X	X	H	Z*

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

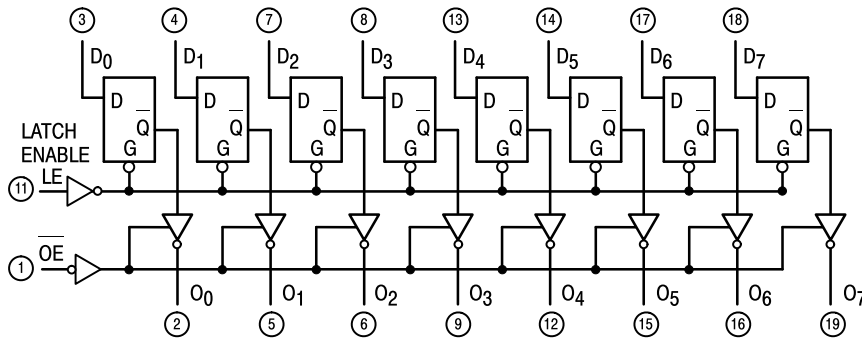
LS374

D <sub>n</sub>	LE	OE	O <sub>n</sub>
H		L	H
L		L	L
X	X	H	Z*

\* Note: Contents of flip-flops unaffected by the state of the Output Enable input (OE).

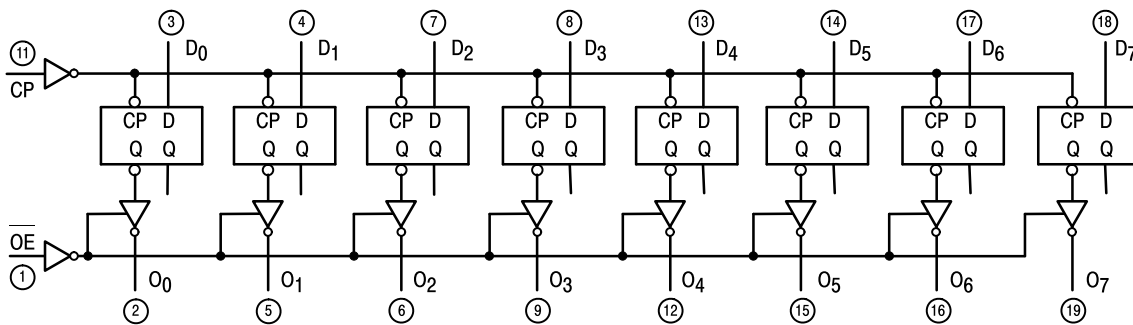
## LOGIC DIAGRAMS

SN54LS/74LS373



V<sub>CC</sub> = PIN 20  
 GND = PIN 10  
 ○ = PIN NUMBERS

SN54LS/74LS374



## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I <sub>OH</sub>	Output Current — High	54 74			-1.0 -2.6	mA
I <sub>OL</sub>	Output Current — Low	54 74			12 24	mA

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## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54	2.4	3.4	V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	
		74	2.4	3.1	V		
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	I <sub>OL</sub> = 12 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V	
I <sub>OZH</sub>	Output Off Current HIGH			20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 2.7 V	
I <sub>OZL</sub>	Output Off Current LOW			-20	μA	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0.4 V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
I <sub>OS</sub>	Short Circuit Current (Note 1)	-30		-130	mA	V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current			40	mA	V <sub>CC</sub> = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS373			LS374				
		Min	Typ	Max	Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency				35	50		MHz	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Data to Output		12 12	18 18				ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Clock or Enable to Output		20 18	30 30		15 19	28 28	ns	
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time		15 25	28 36		20 21	28 28	ns	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time		12 15	20 25		12 15	20 25	ns	C <sub>L</sub> = 5.0 pF

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits				Unit
		LS373		LS374		
		Min	Max	Min	Max	
t <sub>W</sub>	Clock Pulse Width	15		15		ns
t <sub>S</sub>	Setup Time	5.0		20		ns
t <sub>H</sub>	Hold Time	20		0		ns

## DEFINITION OF TERMS

**SETUP TIME (t<sub>S</sub>)** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

**HOLD TIME (t<sub>H</sub>)** — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

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## AC WAVEFORMS

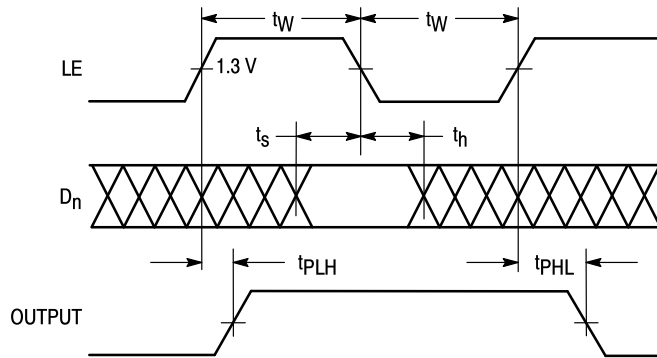


Figure 1

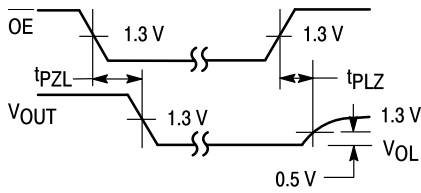


Figure 2

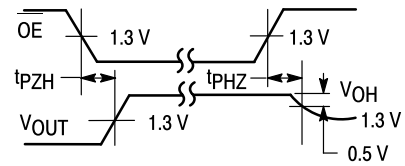
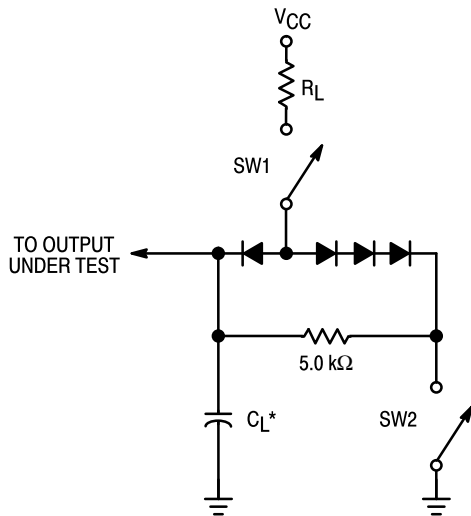


Figure 3

## AC LOAD CIRCUIT



\* Includes Jig and Probe Capacitance.

Figure 4

## SWITCH POSITIONS

SYMBOL	SW1	SW2
$t_{PZH}$	Open	Closed
$t_{PZL}$	Closed	Open
$t_{PLZ}$	Closed	Closed
$t_{PHZ}$	Closed	Closed

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## AC WAVEFORMS

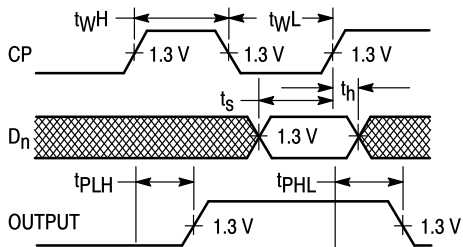


Figure 5

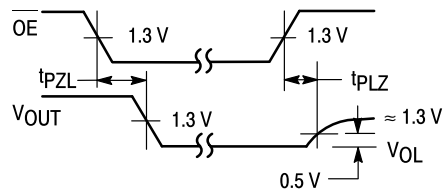


Figure 6

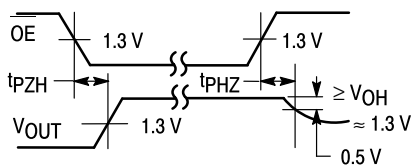
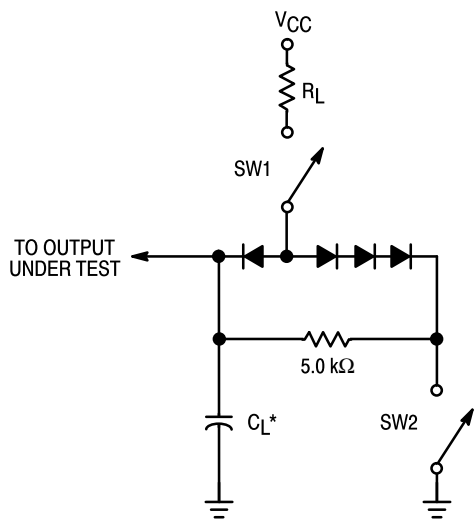


Figure 7

## AC LOAD CIRCUIT



\* Includes Jig and Probe Capacitance.

### SWITCH POSITIONS

SYMBOL	SW1	SW2
tPZH	Open	Closed
tPZL	Closed	Open
tPLZ	Closed	Closed
tPHZ	Closed	Closed

Figure 8



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SYMBOL	SW1	SW2
tpZH	Open	Closed
tpZL	Closed	Open
tpLZ	Closed	Closed

