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NTE74105
Integrated Circuit
TTL – Gated J–K Master–Slave Flip–Flop

Description:

The NTE74105 is a gated J–K master–slave flip–flop in a 14–Lead plastic DIP type package that features a buffered clock input, direct preset and clear, gated J and K inputs, and a common JK input. The clock buffer offers typical TTL high noise immunity, low clock–line loading, and, in most cases, eliminates the need for stringent control of system–clock rise and fall times. When activated, the direct preset and clear inputs control the state of both the master and slave flip–flops independent of the clock and synchronous–input–states. Gated inputs may be used to perform a wide variety of control functions without the need for external gates, and the common JK input simplifies hardware design for applications utilizing a single gate–control source.

Due to the internal clock buffer, the JK input gates accept data when the clock line is low, and transfer of data from the master to the slave occurs during he clock–line transition from the low state to the high state. When the clock line is high, the data inputs are inhibited.

The NTE74105 offers an inverting data input to each of the J and K input gates for additional control flexibility. As the input setup and hold times are not lengthened, this circuit permits operation at higher toggle rates.

Features:

- Buffered Clock Input
- Direct Preset and Clear
- Common JK Gate Input

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 8V
Input Voltage, V_{IN} 5.5V
Voltage Applied to Any Output (Note 2) 5.5V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Voltage values are with respect to network ground terminal.
Note 2. This rating applied at the Q output with preset held low and at the $\overline{Q}$ output with clear held low.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Note 1)	V_{CC}	4.75	5.0	5.25	V
High−Level Input Voltage	V_{OH}	2	–	–	V
Low−Level Input Voltage	V_{OL}	–	–	0.8	V
High−Level Output Current	I_{OH}	–	–	−1	mA
Low−Level Output Current	I_{OL}	–	–	16	mA
Pulse Duration (Note 3) CLK Low−Level	t_w	15	–	_	ns
$\overline{PRE}$ and $\overline{CLR}$		20	–	–	ns
Setup Time for High−Level Data (Note 3, Note 4)	t_{su}	10	–	–	ns
Release Time for Low−Level Data (Note 3, Note 5)	t_h	–	–	1	ns
Operating Temperature Range	T_A	0	–	+70	°C

Note 1. Voltage values are with respect to network ground terminal.
Note 3. These conditions are recommended at V_{CC} = 5V, T_A = +25°C.
Note 4. Setup time for high−level data is an interval between the arrival of the high−level data and the positive−going edge of the clock pulse; this interval being sufficiently long to ensure recognition of the high−level data.
Note 5. Release time for low−level data is an interval between the release of low−level data and the positive−going edge of the clock pulse; this interval being sufficiently short to ensure recognition of the low−level data.

Electrical Characteristics: (Note 6, Note 7)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High−Level Output Voltage	V_{OH}	V_{CC} = MIN, I_{OH} = −1mA	2.4	2.7	–	V
Low−Level Output Voltage	V_{OL}	V_{CC} = MIN, I_{OL} = 16mA	–	0.2	0.4	V
High−Level Input Current $\overline{PRE}$ or $\overline{CLR}$	I_{IH}	V_{CC} = MAX, V_I = 4.5V	–	8	120	μA
J or K			–	4	80	μA
All Other			–	2	40	μA
Low Level Input Current $\overline{PRE}$ or $\overline{CLR}$	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	−3	−4.75	mA
J or K			–	−2.2	−3.2	mA
All Other			–	−1.1	−1.6	mA
Supply Current	I_{CC}	V_{CC} = 5V	–	17	28	mA

Note 6. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.
Note 7. All typical values are at V_{CC} = 5V, T_A = +25°C.
Note 5. Not more than one output should be shorted at a time.
Note 6. I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (From CLK Input to Q or $\overline{Q}$ Output)	t_{PLH}	R_L = 400Ω, C_L = 15pF	–	9	15	ns
	t_{PHL}		–	16	25	ns

Function Table (Each Latch):

Input at t_n			Outputs at t_{n+1}	
JK	**J †**	**K †**	**Q**	**$\overline{Q}$**
L ‡	X	X	Q_n	$\overline{Q}_n$
H	L ‡	L ‡	Q_n	$\overline{Q}_n$
H	L	H	L	H
H	H	L	H	L
H	H	H	$\overline{Q}_n$	Q_n

H = High Level, L = Low Level, X = Irrelevant
t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse
† = J = J1 • $\overline{J2}$ • J3; K = K1 • $\overline{K2}$ • K3
‡ = These low−levels must be maintained while the clock is low.

Pin Connection Diagram