

## DM74LS109A Dual Positive-Edge-Triggered J-K Flip-Flop with Preset, Clear, and Complementary Outputs

### General Description

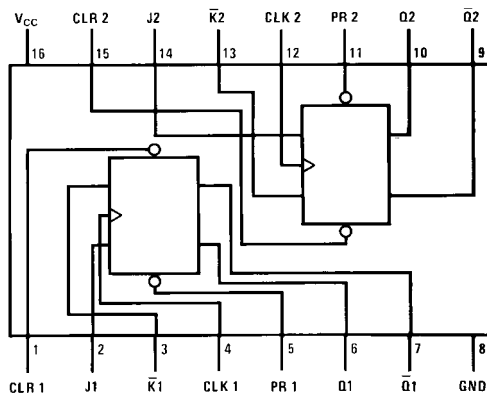
This device contains two independent positive-edge-triggered J-K flip-flops with complementary outputs. The J and K data is accepted by the flip-flop on the rising edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the J and K inputs may be changed while the clock is HIGH or LOW as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

### Ordering Code:

Order Number	Package Number	Package Description
DM74LS109AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS109AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



### Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H (Note 1)	H (Note 1)
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q <sub>0</sub>	Q̄ <sub>0</sub>
H	H	↑	H	H	H	L
H	H	L	X	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

H = HIGH Logic Level

L = LOW Logic Level

X = Either LOW or HIGH Logic Level

↑ = Rising Edge of Pulse

Q<sub>0</sub> = The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each active transition of the clock pulse.

**Note 1:** This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (HIGH) state.

**Absolute Maximum Ratings**(Note 2)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

**Note 2:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
$V_{CC}$	Supply Voltage	4.75	5	5.25	V
$V_{IH}$	HIGH Level Input Voltage	2			V
$V_{IL}$	LOW Level Input Voltage			0.8	V
$I_{OH}$	HIGH Level Output Current			-0.4	mA
$I_{OL}$	LOW Level Output Current			8	mA
$f_{CLK}$	Clock Frequency (Note 3)	0		25	MHz
$f_{CLK}$	Clock Frequency (Note 4)	0		20	MHz
$t_W$	Pulse Width (Note 3)	Clock HIGH	18		ns
		Preset LOW	15		
		Clear LOW	15		
$t_W$	Pulse Width (Note 4)	Clock HIGH	25		ns
		Preset LOW	20		
		Clear LOW	20		
$t_{SU}$	Setup Time (Note 3)(Note 5)	Data HIGH	30 $\uparrow$		ns
		Data LOW	20 $\uparrow$		
$t_{SU}$	Setup Time (Note 5)(Note 4)	Data HIGH	35 $\uparrow$		ns
		Data LOW	25 $\uparrow$		
$t_H$	Hold Time (Note 6)	0 $\uparrow$			ns
$T_A$	Free Air Operating Temperature	0		70	°C

**Note 3:**  $C_L = 15$  pF,  $R_L = 2$  k $\Omega$ ,  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

**Note 4:**  $C_L = 50$  pF,  $R_L = 2$  k $\Omega$ ,  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

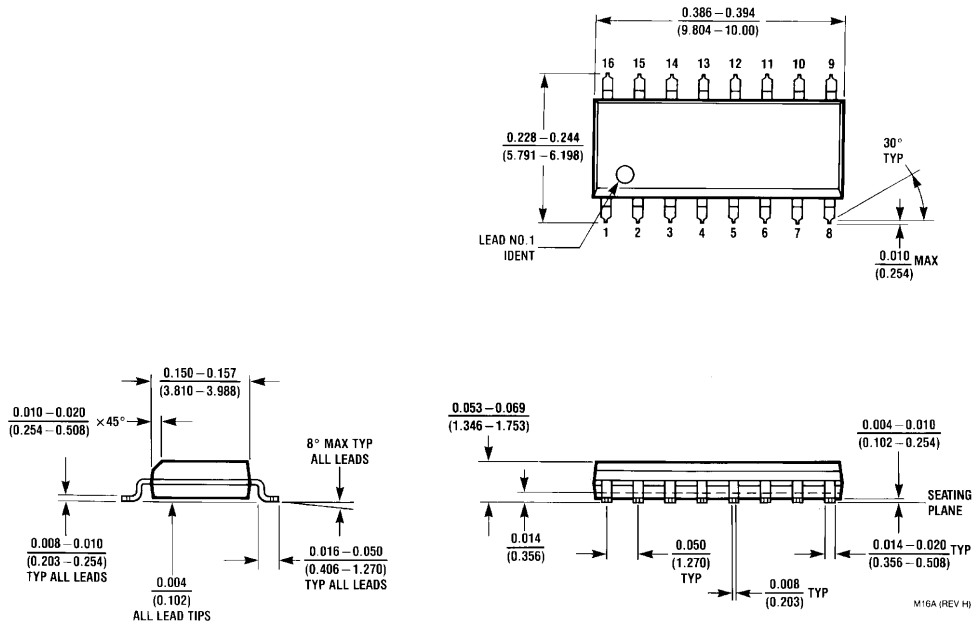
**Note 5:** The symbol ( $\uparrow$ ) indicates the rising edge of the clock pulse is used for reference.

**Note 6:**  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

Electrical Characteristics							
over recommended operating free air temperature range (unless otherwise noted)							
Symbol	Parameter	Conditions	Min	Typ (Note 7)	Max	Units	
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.5	V	
$V_{OH}$	HIGH Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	2.7	3.4		V	
$V_{OL}$	LOW Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$ $I_{OL} = 4 \text{ mA}, V_{CC} = \text{Min}$		0.35 0.25	0.5 0.4	V	
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$ $V_I = 7\text{V}$				mA	
		J, $\bar{K}$			0.1		
		Clock			0.1		
		Preset			0.2		
		Clear			0.2		
$I_{IH}$	HIGH Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.7\text{V}$				$\mu\text{A}$	
		J, $\bar{K}$			20		
		Clock			20		
		Preset			40		
		Clear			40		
$I_{IL}$	LOW Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.4\text{V}$				mA	
		J, $\bar{K}$			-0.4		
		Clock			-0.4		
		Preset			-0.8		
		Clear			-0.8		
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 8)	-20		-100	mA	
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$ (Note 9)		4	8	mA	
<p><b>Note 7:</b> All typicals are at <math>V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}</math>.</p> <p><b>Note 8:</b> Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where <math>V_O = 2.125\text{V}</math> with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.</p> <p><b>Note 9:</b> <math>I_{CC}</math> is measured with all outputs OPEN, with CLOCK grounded after setting the Q and <math>\bar{Q}</math> outputs HIGH in turn.</p>							
Switching Characteristics							
at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$							
Symbol	Parameter	From (Input) To (Output)	$R_L = 2 \text{ k}\Omega$				Units
			$C_L = 15 \text{ pF}$		$C_L = 50 \text{ pF}$		
			Min	Max	Min	Max	
$f_{\text{MAX}}$	Maximum Clock Frequency		25		20		MHz
$t_{\text{PLH}}$	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\bar{Q}$		25		35	ns
$t_{\text{PHL}}$	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\bar{Q}$		30		35	ns
$t_{\text{PLH}}$	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\bar{Q}$		25		35	ns
$t_{\text{PHL}}$	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		30		35	ns
$t_{\text{PLH}}$	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		25		35	ns
$t_{\text{PHL}}$	Propagation Delay Time HIGH-to-LOW Level Output	Preset to $\bar{Q}$		30		35	ns

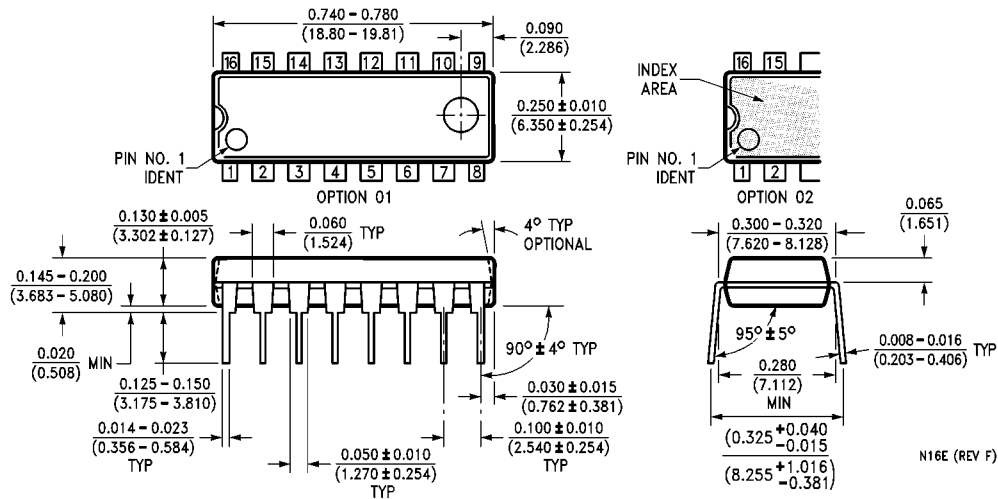
DM74LS109A

**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow  
Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)