8T14
TRIPLE LINE RECEIVER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 8T14 Triple Line Receiver is designed to receive digital information from coaxial cable, strip line, or twisted pair single ended transmission lines. High input impedance (≈30kΩ) presents minimal loading to the transmission lines in multiple receiver applications. The 8T14 has built in hysteresis which makes it ideal for such applications as Schmitt triggers, one-shots, and oscillators. Use the 8T24 triple line receiver where IBM System/360 I/O Interface Specification must be met.

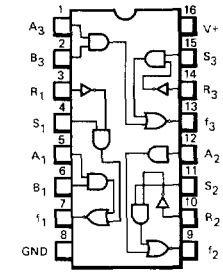
- **BUILT-IN INPUT THRESHOLD HYSTERESIS**
- **HIGH SPEED**
- **INDEPENDENT CHANNEL STROBING**
- **FANOUT OF 10 TTL LOADS**
- **SINGLE +5V SUPPLY OPERATION**

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Note 1)	+5.5V
Output Voltage (Note 1)	+7.0V
Supply Voltage (Note 1)	+7.0V
Storage Temperature Range	
Hermetic DIP (S8T14E, N8T14E)	−65°C to +150°C
Molded DIP (N8T14B)	−55°C to +125°C
Operating Temperature Range	
Military (S8T14)	−55°C to +125°C
Commercial (N8T14)	0°C to +75°C
Lead Temperatures	
Hermetic DIP (soldering, 60 seconds)	300°C
Molded DIP (soldering, 10 seconds)	260°C
Internal Power Dissipation (Note 2)	730mW

NOTES
1. Voltages are with respect to the ground pin (pin 8).
2. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3mW/°C.

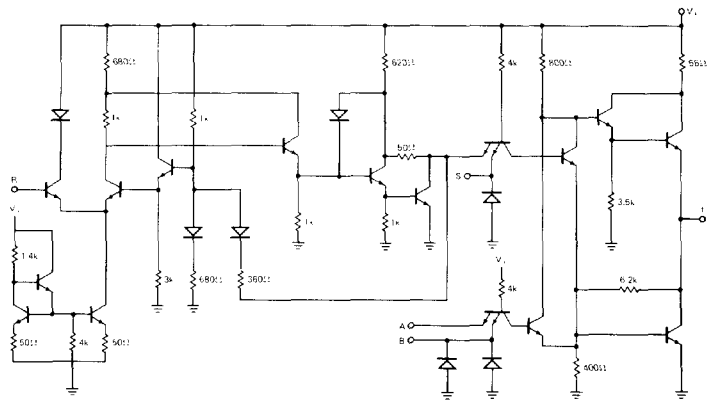
CONNECTION DIAGRAM
16-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6B, 9B



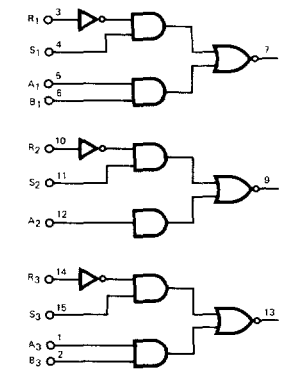
ORDER INFORMATION

TYPE	PART NO.
S8T14	S8T14E
N8T14	N8T14E
N8T14	N8T14B

EQUIVALENT CIRCUIT (EACH RECEIVER)



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (V_+ = 5.0 V ±5%; $-55°C \leq T_A \leq +125°C$ For S8T14 (Note 3)

PARAMETER		TEST CONDITIONS					NOTES	LIMITS			UNITS
		R	S	A	B	OUTPUTS		MIN.	TYP.	MAX.	
Output HIGH Voltage		2.0V	4.5V	0V	0V	−800μA	10,16	2.6	3.5		V
		0V	0.8V	0V	0V	−800μA	10,16	2.6	3.5		V
Output LOW Voltage		0.8V	2.0V	0V	0V	16mA	11,15			0.4	V
		0V	0V	2.0V	2.0V	16mA	11,15			0.4	V
Input LOW Current	S_n	0V	0.4V					−0.1		−1.6	mA
	A_n	0V		0.4V				−0.1		−1.6	mA
	B_n				0.4V			−0.1		−1.6	mA
Input HIGH Current	R_n	3.8V								0.17	mA
	S_n	3.8V	4.5V							40	μA
	A_n			4.5V	0V					40	μA
	B_n			0V	4.5V					40	μA
Hysteresis			4.5V	0V	0V		13,14	0.30	0.50		V

NOTE

3. Specifications apply from 0° C to + 75°C for N8T14.

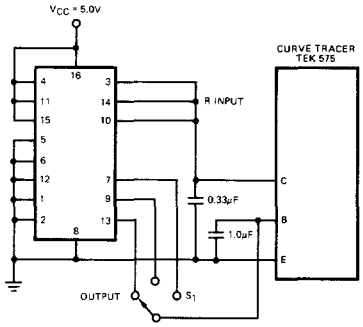
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_+ = 5.0V)

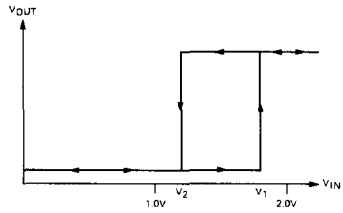
PARAMETER		TEST CONDITIONS					NOTES	LIMITS			UNITS
		R	S	A	B	OUTPUTS		MIN.	TYP.	MAX.	
Turn-on Propagation Delay t_{PHH}		V_{IN}	5.0V	0V	0V		18		20	30	ns
Turn-off Propagation Delay t_{PLL}		V_{IN}	5.0V	0V	0V		18		20	30	ns
Power/Current Consumption									315/60	380/72	mW/mA
Input Voltage Rating	S_n	3.8V	10mA	0V	0V			5.5			V
	A_n	0V	0V	10mA	0V			5.5			V
	B_n	0V	0V	0V	10mA			5.5			V
Output Short-Circuit Current		3.8V	0V	0V	0V	0V		−50		−100	mA
Input Clamp Voltage	S_n		−12mA							−1.5	V
	A_n			−12mA						−1.5	V
	B_n				−12mA					−1.5	V

NOTES

4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. All measurements are taken with ground pin tied to zero volts.
6. Positive current is defined as into the terminal referenced.
7. Positive current flow is defined as into the terminal referenced.
8. Positive Logic Definition: "UP" Level = "HIGH"; "DOWN" Level = "LOW".
9. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the clamp diodes on the S, A, and B inputs become forward biased.
10. Output source current is supplied through a resistor to ground.
11. Output sink current is supplied through a resistor to V_{CC}.
12. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
13. Hysteresis is defined as voltage difference between R input level at which output begins to go from LOW to HIGH state and level at which output begins to go from HIGH to LOW.
14. V_+ = 5.0V.
15. Previous condition is a HIGH output state.
16. Previous condition is a LOW output state.
17. V_+ = 5.25V.
18. Measured as time delay from R input going through 1.5V to the output going through 1.5V. (See 8T24 data sheet ac test circuit).

HYSTERESIS TEST CIRCUIT





Verify in each of three (3) positions of S_1 (Fig. 1) that the following occurs per Fig. 2.

1. V_1 and V_2 must be between 0.8V minimum and 2.0V maximum.
2. Hysteresis = $V_1 - V_2 \geq 0.3V$.

Fig. 1 **Fig. 2**

APPLICATIONS

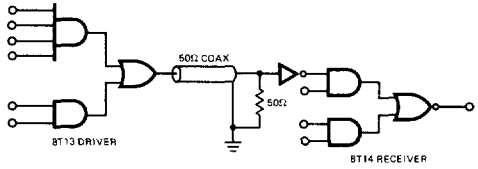
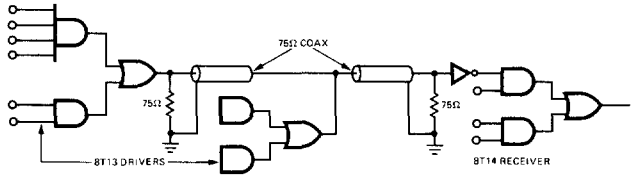


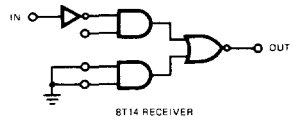
Fig. 3



If more than one driver/receiver pair is to be used on each transmission line, the line should be terminated at both ends as shown in Fig. 4

Fig. 4

SCHMITT TRIGGER APPLICATION



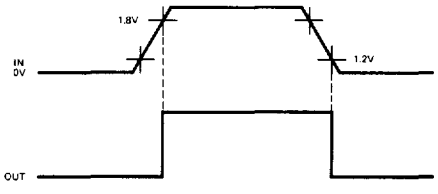


Fig. 5