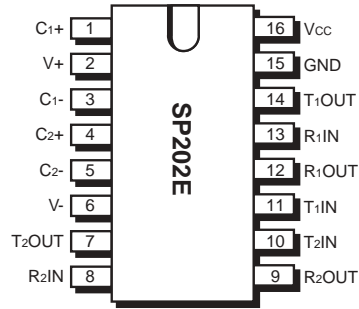




# SP202E/232E/233E/310E/312E

## High-Performance RS-232 Line Drivers/Receivers

- Operates from Single +5V Power Supply
- Meets All RS-232D and ITU V.28 Specifications
- Operates with 0.1µF to 10µF Capacitors
- High Data Rate – 120Kbps Under Load
- Low Power Shutdown  $\leq 1\mu\text{A}$  (Typical)
- 3-State TTL/CMOS Receiver Outputs
- Low Power CMOS – 3mA Operation
- Improved ESD Specifications:
  - ±15kV Human Body Model
  - ±15kV IEC1000-4-2 Air Discharge
  - ±8kV IEC1000-4-2 Contact Discharge



*Now Available in Lead Free Packaging*

### DESCRIPTION

The **SP202E/232E/233E/310E/312E** devices are a family of line driver and receiver pairs that meet the specifications of RS-232 and V.28 serial protocols with enhanced ESD performance. The ESD tolerance has been improved on these devices to over  $\pm 15\text{KV}$  for both Human Body Model and IEC1000-4-2 Air Discharge Method. These devices are pin-to-pin compatible with **Sipex's** SP232A/233A/310A/312A devices as well as popular industry standards. As with the initial versions, the **SP202E/232E/233E/310E/312E** devices feature at least 120Kbps data rate under load, 0.1µF charge pump capacitors, and overall ruggedness for commercial applications. This family also features **Sipex's** BiCMOS design allowing low power operation without sacrificing performance. The series is available in plastic DIP and SOIC packages operating over the commercial and industrial temperature ranges.

### SELECTION TABLE

Model	Number of RS232		No. of Receivers Active in Shutdown	No. of External 0.1µF Capacitors	Shutdown	WakeUp	TTL Tri-State
	Drivers	Receivers					
SP202E	2	2	0	4	No	No	No
SP232E	2	2	0	4	No	No	No
SP233E	2	2	0	0	No	No	No
SP310E	2	2	0	4	Yes	No	Yes
SP312E	2	2	2	4	Yes	Yes	Yes

## ABSOLUTE MAXIMUM RATINGS

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V <sub>CC</sub> .....	+6V
V*.....	(V <sub>CC</sub> -0.3V) to +11.0V
V <sub>-</sub> .....	-11.0V
<b>Input Voltages</b>	
T <sub>IN</sub> .....	-0.3 to (V <sub>CC</sub> +0.3V)
R <sub>IN</sub> .....	±15V
<b>Output Voltages</b>	
T <sub>OUT</sub> .....	(V <sub>+</sub> , +0.3V) to (V <sub>-</sub> , -0.3V)
R <sub>OUT</sub> .....	-0.3V to (V <sub>CC</sub> +0.3V)
<b>Short Circuit Duration</b>	
T <sub>OUT</sub> .....	Continuous

Plastic DIP .....	375mW
(derate 7mW/°C above +70°C)	
Small Outline .....	375mW
(derate 7mW/°C above +70°C)	

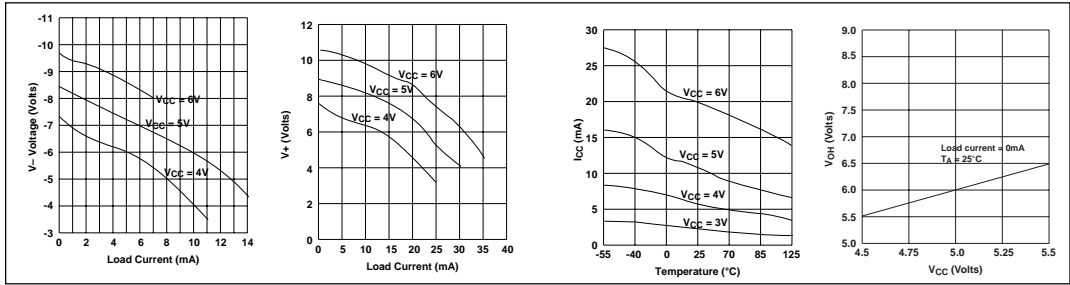
## ELECTRICAL CHARACTERISTICS

V<sub>CC</sub>=+5V±10%; 0.1μF charge pump capacitors; T<sub>MIN</sub> to T<sub>MAX</sub> unless otherwise noted.

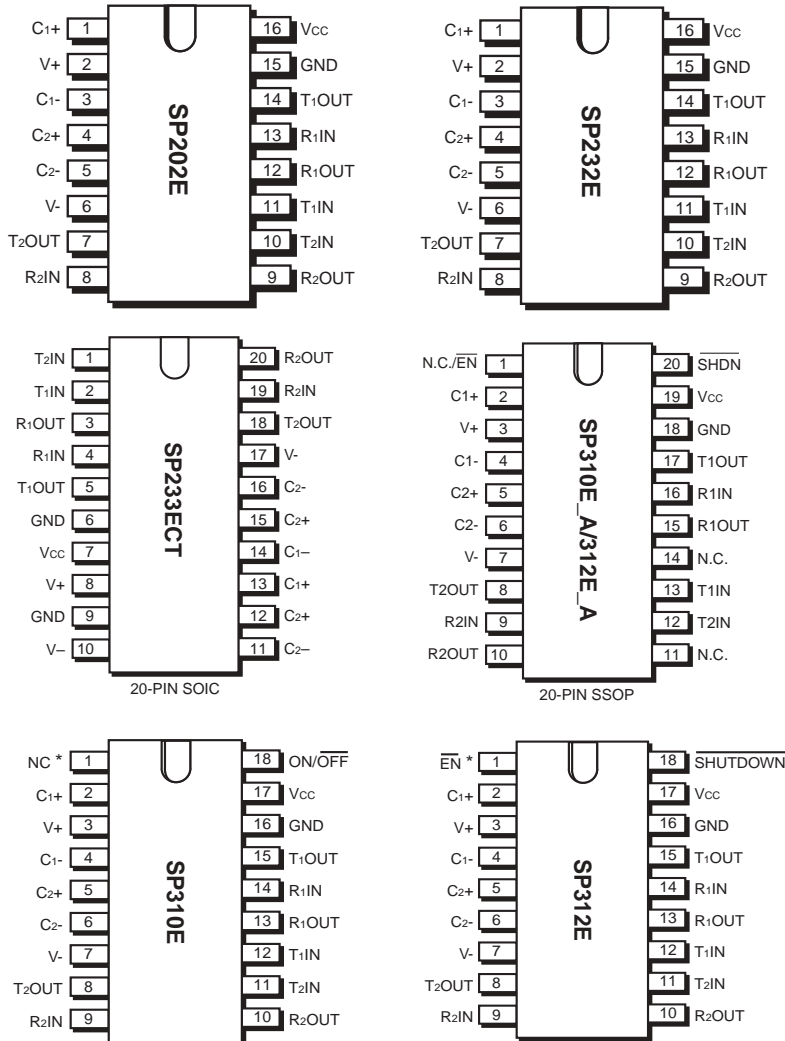
PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>TTL INPUT</b>					
Logic Threshold			0.8	Volts	T <sub>IN</sub> ; $\overline{EN}$ , $\overline{SD}$ T <sub>IN</sub> ; $\overline{EN}$ , $\overline{SD}$ T <sub>IN</sub> = 0V
LOW	2.0			Volts	
HIGH		15	200	μA	
Logic Pull-Up Current					
<b>TTL OUTPUT</b>					
TTL/CMOS Output			0.4	Volts	I <sub>OUT</sub> = 3.2mA; V <sub>CC</sub> = +5V I <sub>OUT</sub> = -1.0mA $\overline{EN} = V_{CC}$ , 0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>
Voltage, Low	3.5			Volts	
Voltage, High		0.05	±10	μA	
Leakage Current **; T <sub>A</sub> = +25°					
<b>RS-232 OUTPUT</b>					
Output Voltage Swing	±5	±6		Volts	All transmitter outputs loaded with 3kΩ to Ground V <sub>CC</sub> = 0V; V <sub>OUT</sub> = ±2V Infinite duration C <sub>L</sub> = 2500pF, R <sub>L</sub> = 3kΩ
Output Resistance	300			Ohms	
Output Short Circuit Current		±18		mA	
Maximum Data Rate	120	240		Kbps	
<b>RS-232 INPUT</b>					
Voltage Range	-15		+15	Volts	V <sub>CC</sub> = 5V, T <sub>A</sub> = +25°C V <sub>CC</sub> = 5V, T <sub>A</sub> = +25°C V <sub>CC</sub> = 5V, T <sub>A</sub> = +25°C T <sub>A</sub> = +25°C, -15V ≤ V <sub>IN</sub> ≤ +15V
Voltage Threshold					
LOW	0.8	1.2		Volts	
HIGH		1.7	2.8	Volts	
Hysteresis	0.2	0.5	1.0	Volts	
Resistance	3	5	7	kΩ	
<b>DYNAMIC CHARACTERISTICS</b>					
Driver Propagation Delay		1.5	3.0	μs	TTL to RS-232; C <sub>L</sub> = 50pF RS-232 to TTL
Receiver Propagation Delay		0.1	1.0	μs	
Instantaneous Slew Rate			30	V/μs	C <sub>L</sub> = 10pF, R <sub>L</sub> = 3-7kΩ; T <sub>A</sub> = +25°C
Transition Region Slew Rate		10		V/μs	C <sub>L</sub> = 2500pF, R <sub>L</sub> = 3kΩ; measured from +3V to -3V or -3V to +3V
Output Enable Time **		400		ns	SP310E and SP312E only
Output Disable Time **		250		ns	SP310E and SP312E only
<b>POWER REQUIREMENTS</b>					
V <sub>CC</sub> Power Supply Current		3	5	mA	No load, T <sub>A</sub> = +25°C; V <sub>CC</sub> = 5V All transmitters R <sub>L</sub> = 3kΩ; T <sub>A</sub> = +25°C
		15		mA	
Shutdown Supply Current **		1	5	μA	V <sub>CC</sub> = 5V, T <sub>A</sub> = +25°C

\*\*SP310E and SP312E only

# PERFORMANCE CURVES



# PINOUTS



\* N.C. for SP310E\_A, EN for SP312E\_A

## FEATURES...

The **SP202E/232E/233E/310E/312E** devices are a family of line driver and receiver pairs that meet the specifications of RS-232 and V.28 serial protocols with enhanced ESD performance. The ESD tolerance has been improved on these devices to over  $\pm 15\text{KV}$  for both Human Body Model and IEC1000-4-2 Air Discharge Method. These devices are pin-to-pin compatible with **Sipex's** 232A/233A/310A/312A devices as well as popular industry standards. As with the initial versions, the **SP202E/232E/233E/310E/312E** devices feature  $10\text{V}/\mu\text{s}$  slew rate,  $120\text{Kbps}$  data rate under load,  $0.1\mu\text{F}$  charge pump capacitors, overall ruggedness for commercial applications, and increased drive current for longer and more flexible cable configurations. This family also features **Sipex's** BiCMOS design allowing low power operation without sacrificing performance.

The **SP202E/232E/233E/310E/312E** devices have internal charge pump voltage converters which allow them to operate from a single  $+5\text{V}$  supply. The charge pumps will operate with polarized or non-polarized capacitors ranging from  $0.1$  to  $10\mu\text{F}$  and will generate the  $\pm 6\text{V}$  needed to generate the RS-232 output levels. Both meet all EIA RS-232 and ITU V.28 specifications.

The **SP310E** provides identical features as the **SP232E** with a single control line which simultaneously shuts down the internal DC/DC converter and puts all transmitter and receiver outputs into a high impedance state. The **SP312E** is identical to the **SP310E** with separate tri-state and shutdown control lines.

## THEORY OF OPERATION

The **SP232E**, **SP233E**, **SP310E** and **SP312E** devices are made up of three basic circuit blocks – 1) a driver/transmitter, 2) a receiver and 3) a charge pump. Each block is described below.

### Driver/Transmitter

The drivers are inverting transmitters, which accept TTL or CMOS inputs and output the RS-232 signals with an inverted sense relative to the input logic levels. Typically the RS-232 output voltage swing is  $\pm 6\text{V}$ . Even under worst case loading conditions of  $3\text{k}\Omega$  and  $2500\text{pF}$ , the output is guaranteed to be  $\pm 5\text{V}$ , which is consistent with the RS-232 standard specifications. The transmitter outputs are protected against infinite short-circuits to ground without degradation in reliability.

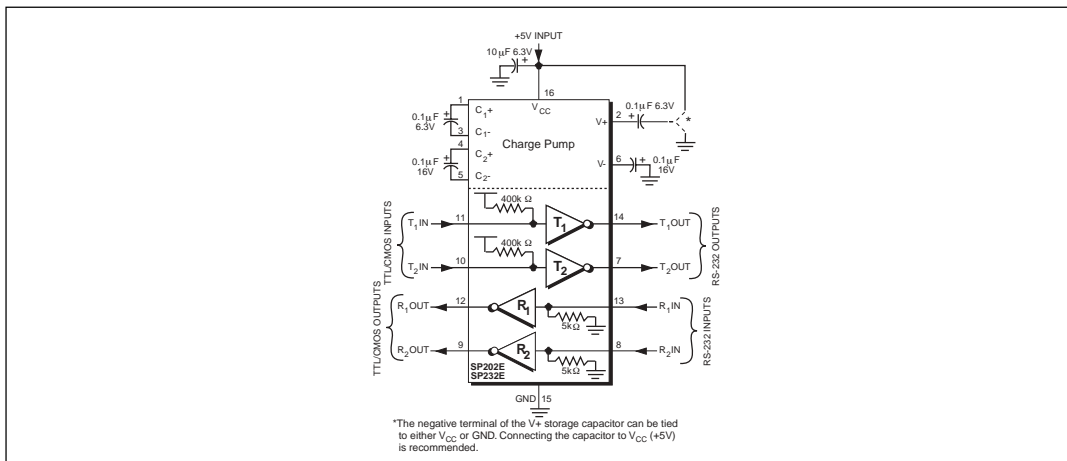


Figure 1. Typical Circuit using the SP202E or SP232E.

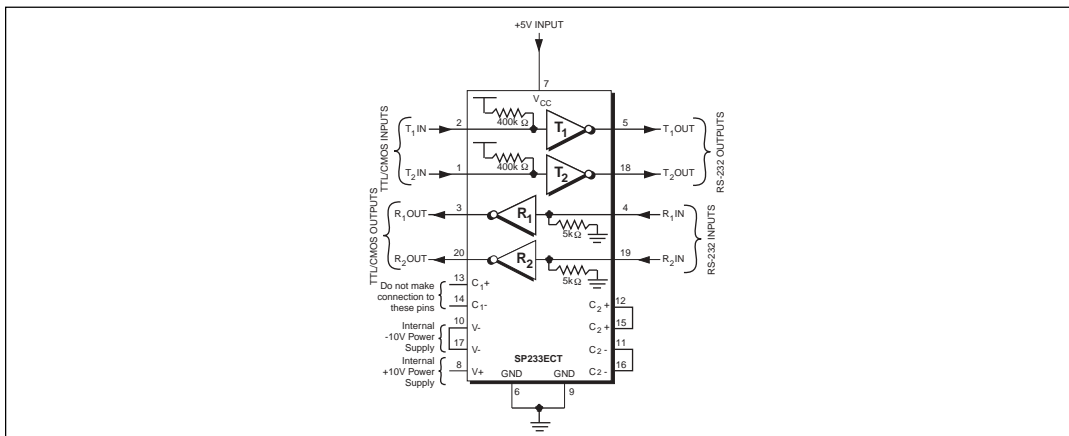


Figure 2. Typical Circuits using the SP233ECP and SP233ECT

The instantaneous slew rate of the transmitter output is internally limited to a maximum of 30V/ $\mu$ s in order to meet the standards [EIA RS-232-D 2.1.7, Paragraph (5)]. However, the transition region slew rate of these enhanced products is typically 10V/ $\mu$ s. The smooth transition of the loaded output from  $V_{OL}$  to  $V_{OH}$  clearly meets the monotonicity requirements of the standard [EIA RS-232-D 2.1.7, Paragraphs (1) & (2)].

### Receivers

The receivers convert RS-232 input signals to inverted TTL signals. Since the input is usually from a transmission line, where long cable lengths

and system interference can degrade the signal, the inputs have a typical hysteresis margin of 500mV. This ensures that the receiver is virtually immune to noisy transmission lines.

The input thresholds are 0.8V minimum and 2.4V maximum, again well within the  $\pm 3V$  RS-232 requirements. The receiver inputs are also protected against voltages up to  $\pm 15V$ . Should an input be left unconnected, a 5KOhm pull-down resistor to ground will commit the output of the receiver to a high state.

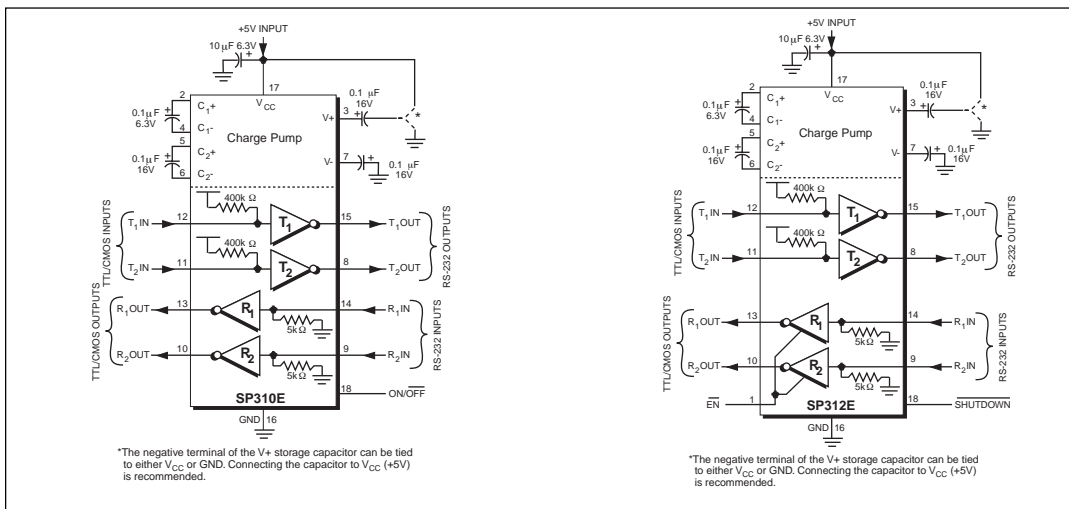


Figure 3. Typical Circuits using the SP310E and SP312E

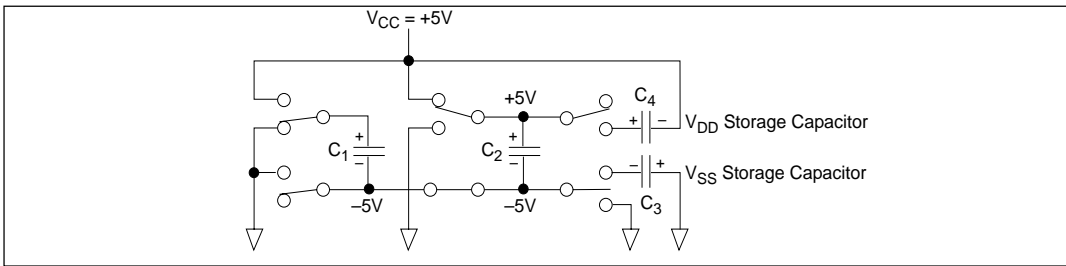


Figure 4. Charge Pump — Phase 1

In actual system applications, it is quite possible for signals to be applied to the receiver inputs before power is applied to the receiver circuitry. This occurs, for example, when a PC user attempts to print, only to realize the printer wasn't turned on. In this case an RS-232 signal from the PC will appear on the receiver input at the printer. When the printer power is turned on, the receiver will operate normally. All of these enhanced devices are fully protected.

### Charge Pump

The charge pump is a Sipex-patented design (5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical power supplies. There is a free-running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

#### Phase 1

—  $V_{SS}$  charge storage — During this phase of the clock cycle, the positive side of capacitors  $C_1$  and  $C_2$  are initially charged to +5V.  $C_1^+$  is then switched to ground and the charge in  $C_1^-$  is transferred to  $C_2^-$ . Since  $C_2^+$  is connected to +5V, the voltage potential across capacitor  $C_2$  is now 10V.

#### Phase 2

—  $V_{SS}$  transfer — Phase two of the clock connects the negative terminal of  $C_2$  to the  $V_{SS}$  storage capacitor and the positive terminal of  $C_2$  to ground, and transfers the generated -10V to  $C_3$ . Simultaneously, the positive side of capacitor  $C_1$  is switched to +5V and the negative side is connected to ground.

#### Phase 3

—  $V_{DD}$  charge storage — The third phase of the clock is identical to the first phase — the charge transferred in  $C_1$  produces -5V in the negative terminal of  $C_1$ , which is applied to the negative side of capacitor  $C_2$ . Since  $C_2^+$  is at +5V, the voltage potential across  $C_2$  is 10V.

#### Phase 4

—  $V_{DD}$  transfer — The fourth phase of the clock connects the negative terminal of  $C_2$  to ground, and transfers the generated 10V across  $C_2$  to  $C_4$ , the  $V_{DD}$  storage capacitor. Again, simultaneously with this, the positive side of capacitor  $C_1$  is connected to +5V and the negative side is connected to ground, and the cycle begins again.

Since both  $V^+$  and  $V^-$  are separately generated from  $V_{CC}$ ; in a no-load condition  $V^+$  and  $V^-$  will

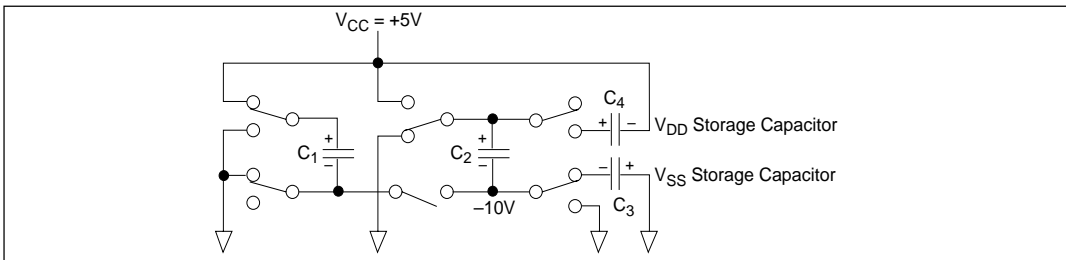


Figure 5. Charge Pump — Phase 2

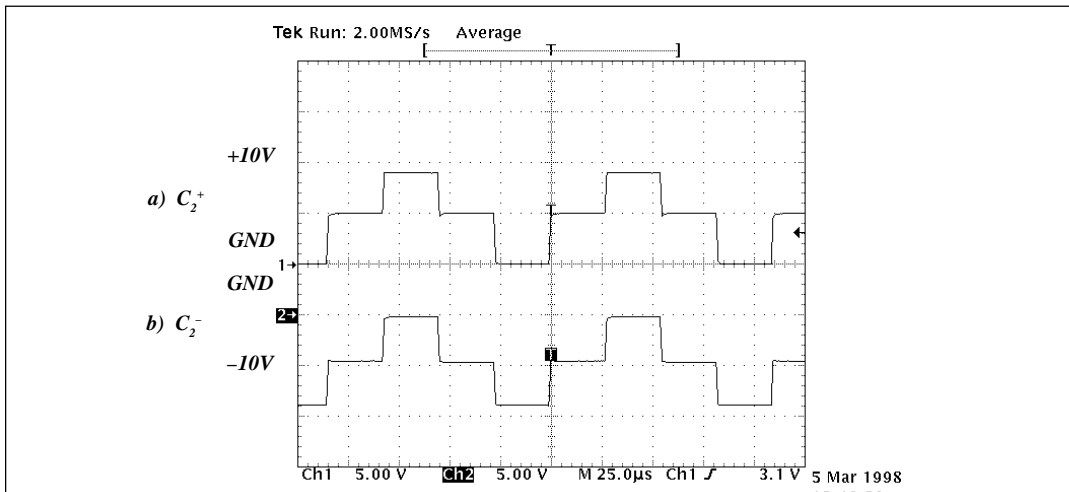


Figure 6. Charge Pump Waveforms

be symmetrical. Older charge pump approaches that generate  $V^-$  from  $V^+$  will show a decrease in the magnitude of  $V^-$  compared to  $V^+$  due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors can be as low as  $0.1\mu\text{F}$  with a 16V breakdown voltage rating.

### Shutdown ( $\overline{\text{SD}}$ ) and Enable ( $\overline{\text{EN}}$ ) for the SP310E and SP312E

Both the **SP310E** and **SP312E** have a shutdown/standby mode to conserve power in battery-powered systems. To activate the shutdown mode, which stops the operation of the charge pump, a logic “0” is applied to the appropriate control line. For the **SP310E**, this control line is  $\text{ON}/\overline{\text{OFF}}$  (pin 18). Activating the shutdown mode also puts the

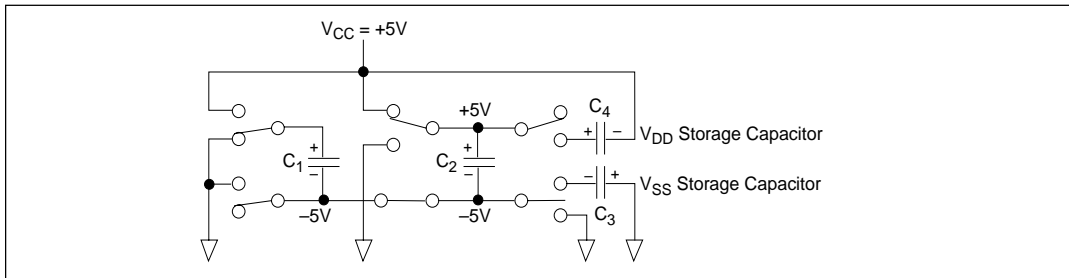


Figure 7. Charge Pump — Phase 3

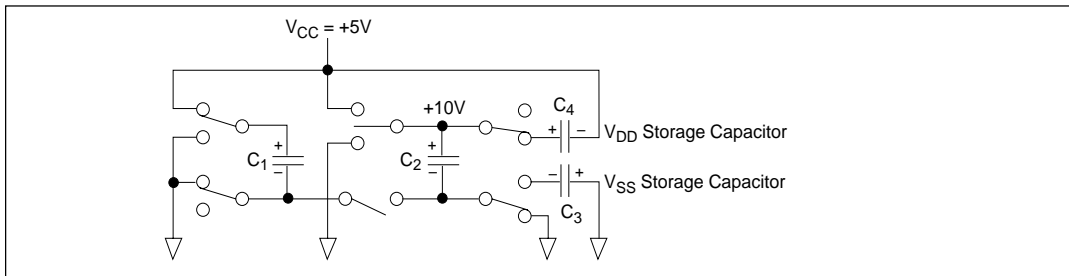


Figure 8. Charge Pump — Phase 4

**SP310E** transmitter and receiver outputs in a high impedance condition (tri-stated). The shutdown mode is controlled on the **SP312E** by a logic “0” on the **SHUTDOWN** control line (pin 18); this also puts the transmitter outputs in a tri-state mode. The receiver outputs can be tri-stated separately during normal operation or shutdown by a logic “1” on the **ENABLE** line (pin 1).

### Wake-Up Feature for the SP312E

The **SP312E** has a wake-up feature that keeps all the receivers in an enabled state when the device is in the shutdown mode. *Table 1* defines the truth table for the wake-up function.

With only the receivers activated, the **SP312E** typically draws less than 5 $\mu$ A supply current. In the case of a modem interfaced to a computer in power down mode, the Ring Indicator (RI) signal from the modem would be used to "wake up" the computer, allowing it to accept data transmission.

After the ring indicator signal has propagated through the **SP312E** receiver, it can be used to trigger the power management circuitry of the computer to power up the microprocessor, and bring the **SD** pin of the **SP312E** to a logic high, taking it out of the shutdown mode. The receiver propagation delay is typically 1 $\mu$ s. The enable time for V<sup>+</sup> and V<sup>-</sup> is typically 2ms. After V<sup>+</sup> and V<sup>-</sup> have settled to their final values, a signal can be sent back to the modem on the data terminal ready (DTR) pin signifying that the computer is ready to accept and transmit data.

<b>SD</b>	<b>EN</b>	<b>Power Up/Down</b>	<b>Receiver Outputs</b>
0	0	Down	Enable
0	1	Down	Tri-state
1	0	Up	Enable
1	1	Up	Tri-state

*Table 1. Wake-up Function Truth Table.*

### Pin Strapping for the SP233ECT

The **SP233E** packaged in the 20-pin SOIC package (**SP233ECT**) has a slightly different pinout than the **SP233E** in other package configurations. To operate properly, the following pairs of pins must be externally wired together:

- the two V<sup>-</sup> pins (pins 10 and 17)
- the two C<sub>2+</sub> pins (pins 12 and 15)
- the two C<sub>2-</sub> pins (pins 11 and 16)

All other connections, features, functions and performance are identical to the **SP233E** as specified elsewhere in this data sheet.

### ESD TOLERANCE

The **SP202E/232E/233E/310E/312E** devices incorporate ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least  $\pm 15$ KV without damage nor latch-up.

There are different methods of ESD testing applied:

- a) MIL-STD-883, Method 3015.7
- b) IEC1000-4-2 Air-Discharge
- c) IEC1000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in *Figure 9*. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-1000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise



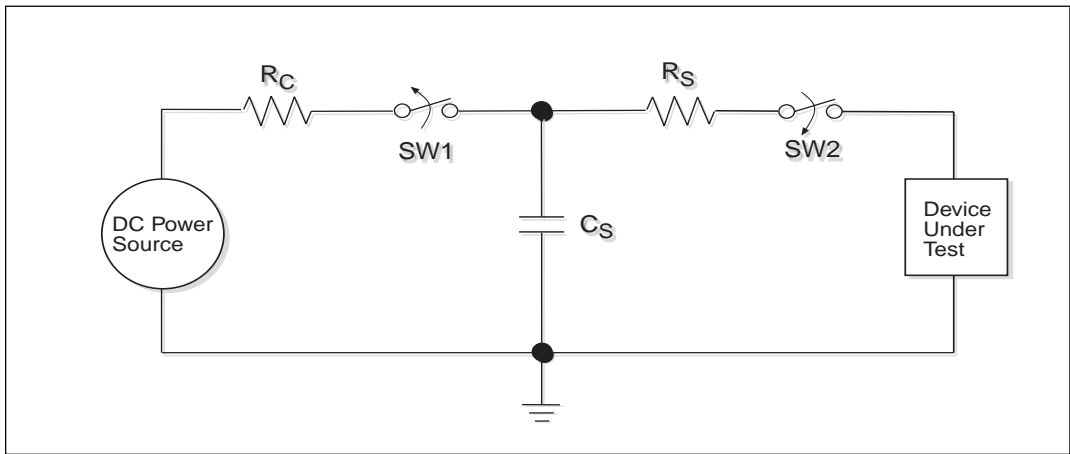


Figure 9. ESD Test Circuit for Human Body Model

with IEC1000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC1000-4-2 is shown on Figure 10. There are two methods within IEC1000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the

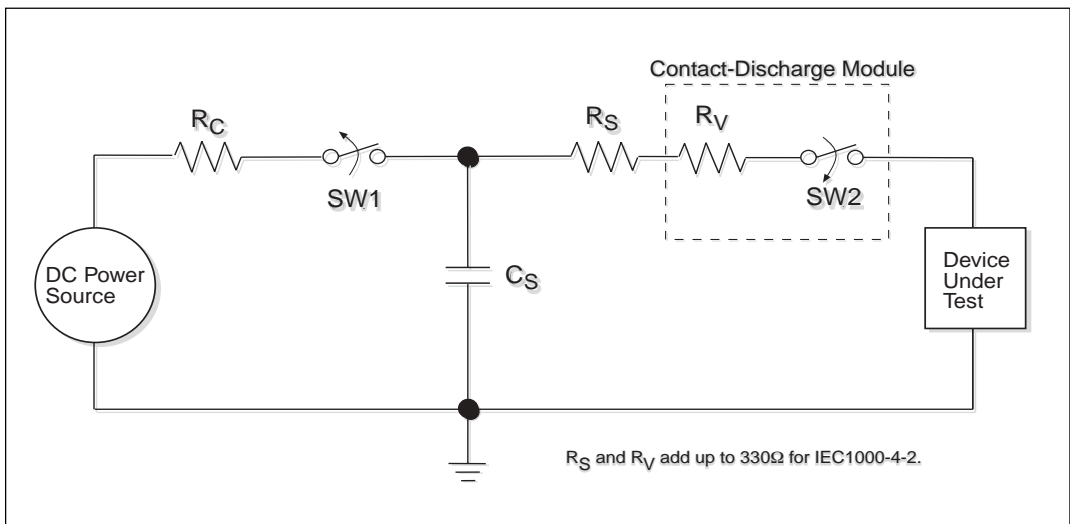


Figure 10. ESD Test Circuit for IEC1000-4-2

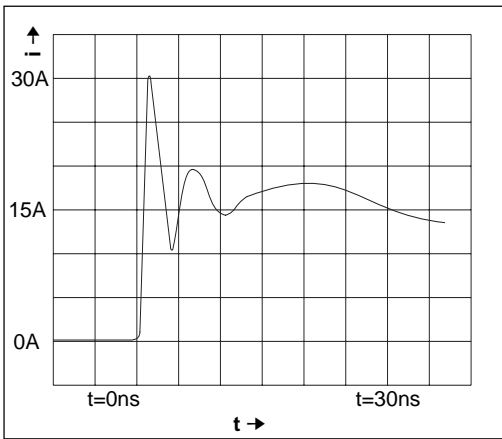


Figure 11. ESD Test Waveform for IEC1000-4-2

discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly

discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

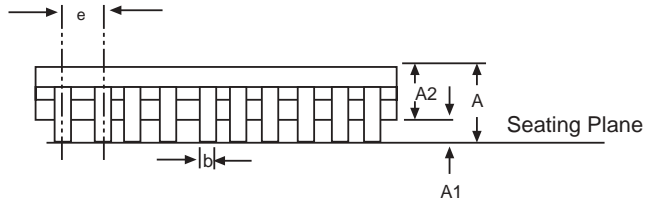
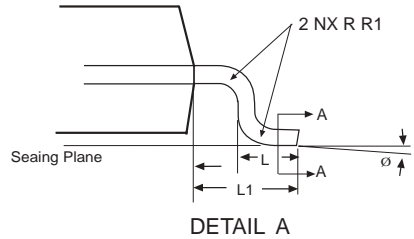
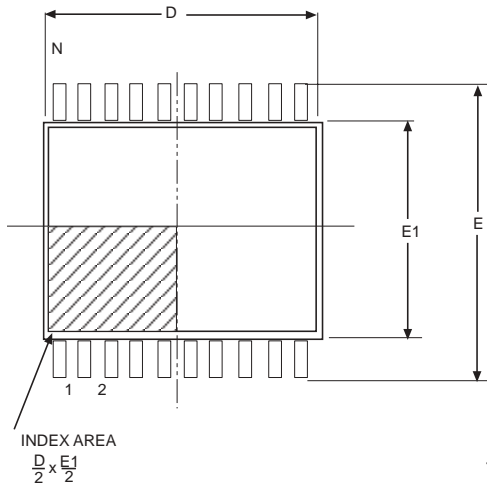
The circuit models in Figures 9 and 10 represent the typical ESD testing circuit used for all three methods. The  $C_S$  is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through  $R_S$ , the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor ( $R_S$ ) and the source capacitor ( $C_S$ ) are  $1.5k\Omega$  and  $100pF$ , respectively. For IEC-1000-4-2, the current limiting resistor ( $R_S$ ) and the source capacitor ( $C_S$ ) are  $330\Omega$  and  $150pF$ , respectively.

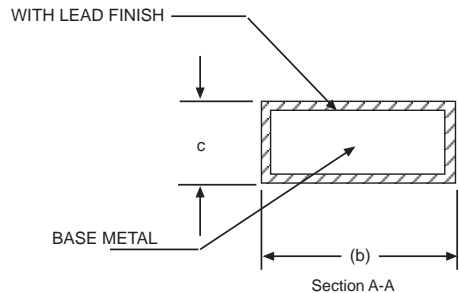
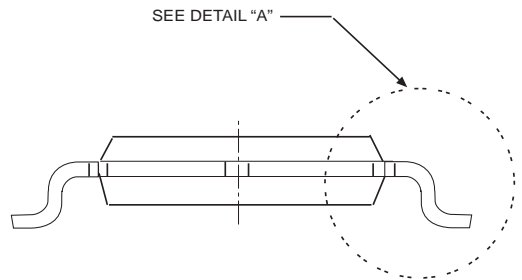
The higher  $C_S$  value and lower  $R_S$  value in the IEC1000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

SP202E Family	HUMAN BODY MODEL	IEC1000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	$\pm 15kV$	$\pm 15kV$	$\pm 8kV$	4
Receiver Inputs	$\pm 15kV$	$\pm 15kV$	$\pm 8kV$	4

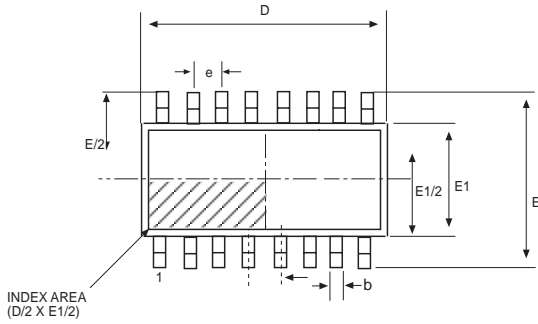
Table 2. Transceiver ESD Tolerance Levels



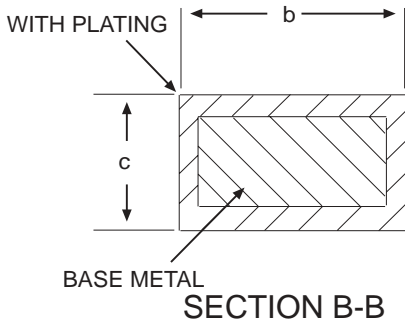
20 PIN SSOP JEDEC MO-150 (AE) Variation	Dimensions in (mm)		
	MIN	NOM	MAX
A	-	-	2.0
A1	0.05	-	-
A2	1.65	1.75	1.85
b	0.22	-	0.38
c	0.09	-	0.25
D	6.90	7.20	7.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
L	0.55	0.75	0.95
L1	1.25 REF		
∅	0°	4°	8°



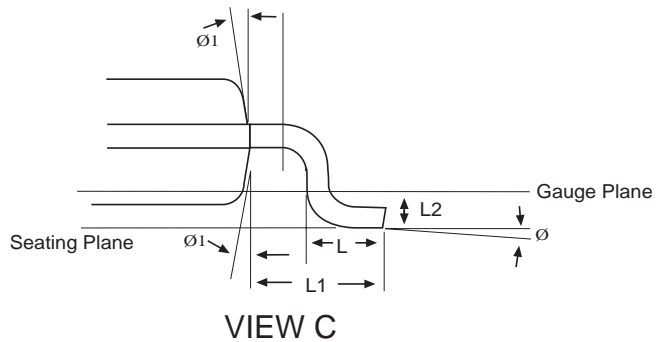
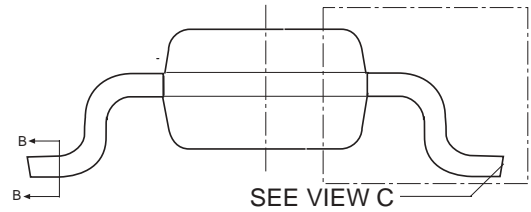
20 PIN SSOP



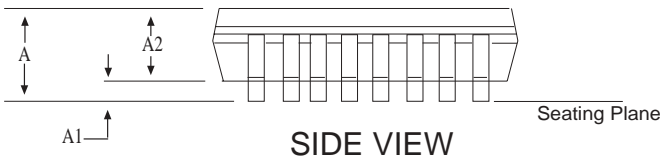
TOP VIEW



SECTION B-B



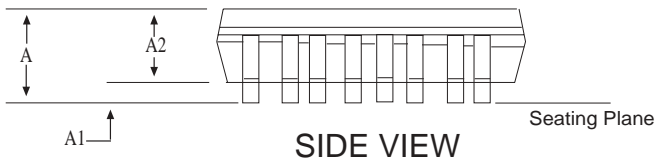
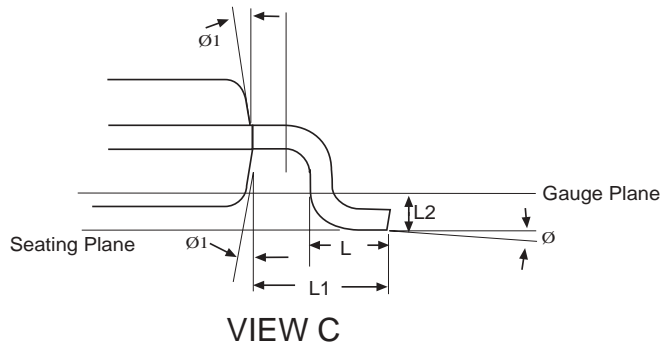
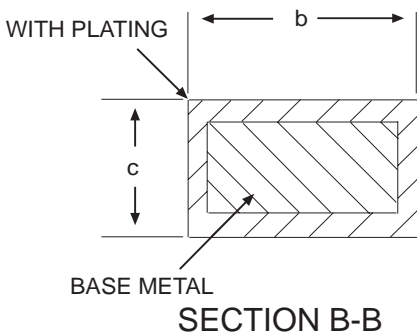
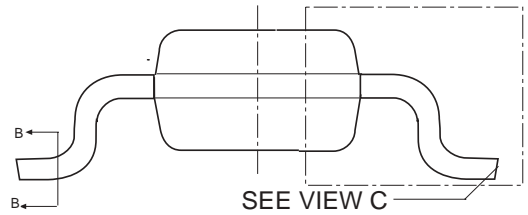
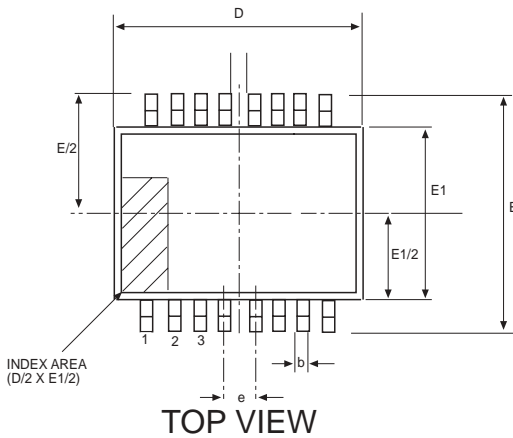
VIEW C



SIDE VIEW

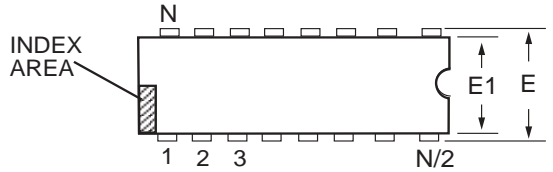
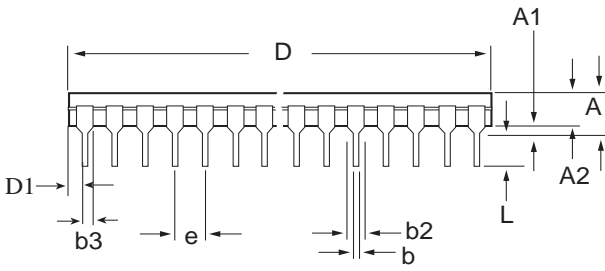
16 Pin NSOIC (JEDEC MS-012, AC - VARIATION)	DIMENSIONS in (mm)			
	SYMBOL	MIN	NOM	MAX
	A	1.35	-	1.75
	A1	0.10	-	0.25
	A2	1.25	-	1.65
	b	0.31	-	0.51
	c	0.17	-	0.25
	D	9.90 BSC		
	E	6.00 BSC		
	E1	3.90 BSC		
	e	1.27 BSC		
	L	0.40	-	1.27
	L1	1.04 REF		
	L2	0.25 BSC		
	Ø	0°	-	8°
	Ø1	5°	-	15°

16 PIN NSOIC

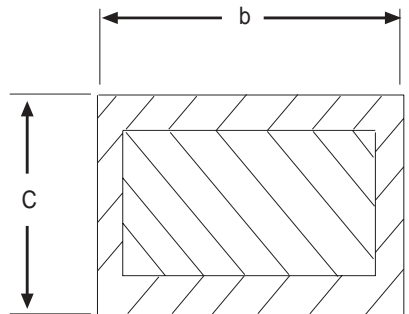
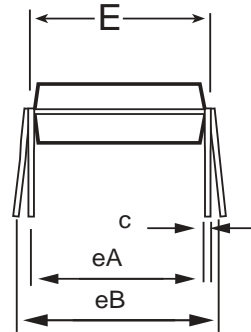


16 Pin SOIC (WIDE) (JEDEC MS-013 AA - VARIATION)	DIMENSIONS IN (mm)		
SYMBOL	MIN	NOM	MAX
A	2.35	-	2.65
A1	0.10	-	0.30
A2	2.05	-	2.55
b	0.31	-	0.51
c	0.20	-	0.33
D	10.30 BSC		
E	10.30 BSC		
E1	7.50 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.40 REF		
L2	0.25 BSC		
Ø	0°	-	8°
Ø1	5°	-	15°

**16 PIN SOIC WIDE**



18 PIN PDIP JEDEC MS-001 (AC) Variation	Dimensions in inches		
	MIN	NOM	MAX
A	-	-	.210
A1	.015	-	-
A2	.115	.130	.195
b	.014	.018	.022
b2	.045	.060	.070
b3	.030	.039	.045
c	.008	.010	.014
D	.880	.900	.920
D1	.005	-	-
E	.300	.310	.325
E1	.240	.250	.280
e	.100 BSC		
eA	.300 BSC		
eB	-	-	.430
L	.115	.130	.150



18 pin PDIP

Part Number	Temperature Range	Topmark	Package
SP202ECN.....	0°C to +70°C.....	SP202ECN.....	16-pin NSOIC
SP202ECN/TR.....	0°C to +70°C.....	SP202ECN.....	16-pin NSOIC
SP202ECP.....	0°C to +70°C.....	SP202ECP.....	16-pin PDIP
SP202ECT.....	0°C to +70°C.....	SP202ECT.....	16-pin WSOIC
SP202ECT/TR.....	0°C to +70°C.....	SP202ECT.....	16-pin WSOIC
SP202EEN.....	-40°C to +85°C.....	SP202EEN.....	16-pin NSOIC
SP202EEN/TR.....	-40°C to +85°C.....	SP202EEN.....	16-pin NSOIC
SP202EET.....	-40°C to +85°C.....	SP202EET.....	16-pin PDIP
SP202EET.....	-40°C to +85°C.....	SP202EET.....	16-pin WSOIC
SP202EET/TR.....	-40°C to +85°C.....	SP202EET.....	16-pin WSOIC
SP232ECN.....	0°C to +70°C.....	SP232ECN.....	16-pin NSOIC
SP232ECN/TR.....	0°C to +70°C.....	SP232ECN.....	16-pin NSOIC
SP232ECP.....	0°C to +70°C.....	SP232ECP.....	16-pin PDIP
SP232ECT.....	0°C to +70°C.....	SP232ECT.....	16-pin WSOIC
SP232ECT/TR.....	0°C to +70°C.....	SP232ECT.....	16-pin WSOIC
SP232EEN.....	-40°C to +85°C.....	SP232EEN.....	16-pin NSOIC
SP232EEN/TR.....	-40°C to +85°C.....	SP232EEN.....	16-pin NSOIC
SP232EET.....	-40°C to +85°C.....	SP232EET.....	16-pin PDIP
SP232EET.....	-40°C to +85°C.....	SP232EET.....	16-pin WSOIC
SP232EET/TR.....	-40°C to +85°C.....	SP232EET.....	16-pin WSOIC
SP233ECT.....	0°C to +70°C.....	SP233ECT.....	20-pin WSOIC
SP233ECT/TR.....	0°C to +70°C.....	SP233ECT.....	20-pin WSOIC
SP233EET.....	-40°C to +85°C.....	SP233EET.....	20-pin WSOIC
SP233EET/TR.....	-40°C to +85°C.....	SP233EET.....	20-pin WSOIC
SP310ECP.....	0°C to +70°C.....	SP310ECP.....	18-pin PDIP
SP310ECT.....	0°C to +70°C.....	SP310ECT.....	18-pin WSOIC
SP310ECT/TR.....	0°C to +70°C.....	SP310ECT.....	18-pin WSOIC
SP310ECA.....	0°C to +70°C.....	SP310ECA.....	20-pin SSOP
SP310ECA/TR.....	0°C to +70°C.....	SP310ECA.....	20-pin SSOP
SP310EEP.....	-40°C to +85°C.....	SP310EEP.....	18-pin PDIP
SP310EET.....	-40°C to +85°C.....	SP310EET.....	18-pin WSOIC
SP310EET/TR.....	-40°C to +85°C.....	SP310EET.....	18-pin WSOIC
SP310EEA.....	-40°C to +85°C.....	SP310EEA.....	20-pin SSOP
SP310EEA/TR.....	-40°C to +85°C.....	SP310EEA.....	20-pin SSOP
SP312ECP.....	0°C to +70°C.....	SP312ECP.....	18-pin PDIP
SP312ECT.....	0°C to +70°C.....	SP312ECT.....	18-pin WSOIC
SP312ECT/TR.....	0°C to +70°C.....	SP312ECT.....	18-pin WSOIC
SP312ECA.....	0°C to +70°C.....	SP312ECA.....	20-pin SSOP
SP312ECA/TR.....	0°C to +70°C.....	SP312ECA.....	20-pin SSOP
SP312EEP.....	-40°C to +85°C.....	SP312EEP.....	18-pin PDIP
SP312EET.....	-40°C to +85°C.....	SP312EET.....	18-pin WSOIC
SP312EET/TR.....	-40°C to +85°C.....	SP312EET.....	18-pin WSOIC
SP312EEA.....	-40°C to +85°C.....	SP312EEA.....	20-pin SSOP
SP312EEA/TR.....	-40°C to +85°C.....	SP312EEA.....	20-pin SSOP

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP312EEA/TR = standard; SP312EEA-L/TR = lead free

/TR = Tape and Reel

Pack quantity is 1,500 for SSOP or WSOIC and 2,500 for NSOIC.

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**REVISION HISTORY**

DATE	REVISION	DESCRIPTION
6/2/04	A	Incorporated new package drawings with JEDEC reference.
7/19/04	A	Added typical output voltage swing value (±6V).

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