UC200T

Hardware Design

UMTS/HSPA+ Module Series

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About the Document

History

Revision	Date	Author	Description
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1 Introduction

This document defines UC200T module and describes its air interface and hardware interface which are connected with customers' applications.

This document helps customers quickly understand module interface specifications, electrical and mechanical details, as well as other related information of UC200T module. Associated with application note and user guide, customers can use UC200T module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating UC200T module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

UC200T is a WCDMA/GSM wireless communication module. Its general features are listed below：

- Support HSDPA, HSUPA, HSPA+, WCDMA, EDGE, GSM and GPRS coverage.
- Provide audio support for customers' specific applications.

UC200T is available in two variants: UC200T-EM and UC200T-GL. The supported frequency bands of UC200T are shown in the following tables.

Table 1: UC200T-EM Frequency Bands

Type	Frequency Bands
WCDMA	B1/B8
GSM	900/1800MHz

Table 2: UC200T-GL Frequency Bands

Type	Frequency Bands
WCDMA	B1/B2/B5/B6/B8
GSM	850/900/1800/1900MHz

UC200T is an SMD-type module which can be embedded in applications through its 144 pins (including 80 LCC pins and 64 LGA pins). With a compact profile of 29.0mm × 32.0mm × 2.4mm, it can meet almost all requirements for M2M applications such as automotive, metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC and etc.

2.2. Key Features

The following table describes the detailed features of UC200T module.

Table 3: Key Features of UC200T Module

Feature	Details
Power Supply	Supply voltage: 3.4V~4.5V Typical supply voltage: 3.8V
Transmitting Power	Class 4 (33dBm±2dB) for GSM850/EGSM900 Class 1 (30dBm±2dB) for DCS1800/PCS1900 Class E2 (27dBm±3dB) for GSM850/EGSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800/PCS1900 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands
UMTS Features	Support 3GPP R7 HSDPA, HSPA+, HSUPA and WCDMA Support QPSK, 16-QAM modulation HSPA+: Max 21Mbps (DL) HSUPA: Max 5.76Mbps (UL) WCDMA: Max 384Kbps (DL), Max 384Kbps (UL)
GSM Features	**GPRS** ● Support GPRS multi-slot class 12 ● Coding schemes: CS-1, CS-2, CS-3 and CS-4 ● Max 85.6Kbps (DL), Max 85.6Kbps (UL) **EDGE** ● Support EDGE multi-slot class 12 ● Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) ● Downlink coding schemes: CS 1-4 and MCS 1-9 ● Uplink coding schemes: CS 1-4 and MCS 1-9 ● Max 236.8Kbps (DL), Max 236.8Kbps (UL)
Internet Protocol Features	Support TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/FTPS/SSL/FILE/MQTT/SMTP*/MMS*/SMTPS* protocols Support PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) protocols which as usually used for PPP connection
SMS	Text and PDU modes Point-to-point MO and MT SMS cell broadcast SMS storage: (U)SIM card currently
USIM Interface	Support USIM/SIM card: 1.8V/3.0V

Audio Features	Support one digital audio interface: PCM interface GSM: HR/FR/EFR/AMR/AMR-WB WCDMA: AMR/AMR-WB Support echo cancellation and noise suppression
PCM Interface	Used for audio function with an external codec chip Support 16-bit linear data format Support short frame synchronization Support master and slave modes
USB Interface	Compliant with USB 2.0 specification (slave only), with transmission rates up to 480Mbps Used for AT command communication, data transmission, software debugging and firmware upgrade Support USB serial drivers for: ● Windows 7/8/8.1/10 ● Windows CE 5.0/6.0/7.0* ● Linux 2.6~5.0 ● Android 4.x/5.x/6.x/7.x/8.x/9.x
UART Interface	**Main UART** ● Used for AT command communication and data transmission ● Baud rate reach up to 1Mbps; 115200bps by default ● Support RTS and CTS hardware flow control **Debug UART** ● Used for Linux console, log output ● 115200bps baud rate
SD Card Interface*	Support SD3.0 protocol
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Network Indication	NET_MODE and NET_STATUS are used to indicate the network connectivity status
Antenna Interface	Main antenna interface (ANT_MAIN)
Physical Characteristics	Size: (29.0±0.15)mm × (32.0±0.15)mm × (2.4±0.2)mm Weight: approx. 4.3g
Temperature Range	Operation temperature range: -35°C ~ +75°C [1)] Extended temperature range: -40°C ~ +85°C [2)] Storage temperature range: -40°C ~ +90°C
Firmware Upgrade	USB interface and FOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1] Within the operation temperature range, the module is 3GPP compliant.
2. [2] Within the extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of UC200T and illustrates the major functional parts.

- Power management
- Baseband
- Flash
- Radio frequency
- Peripheral interfaces

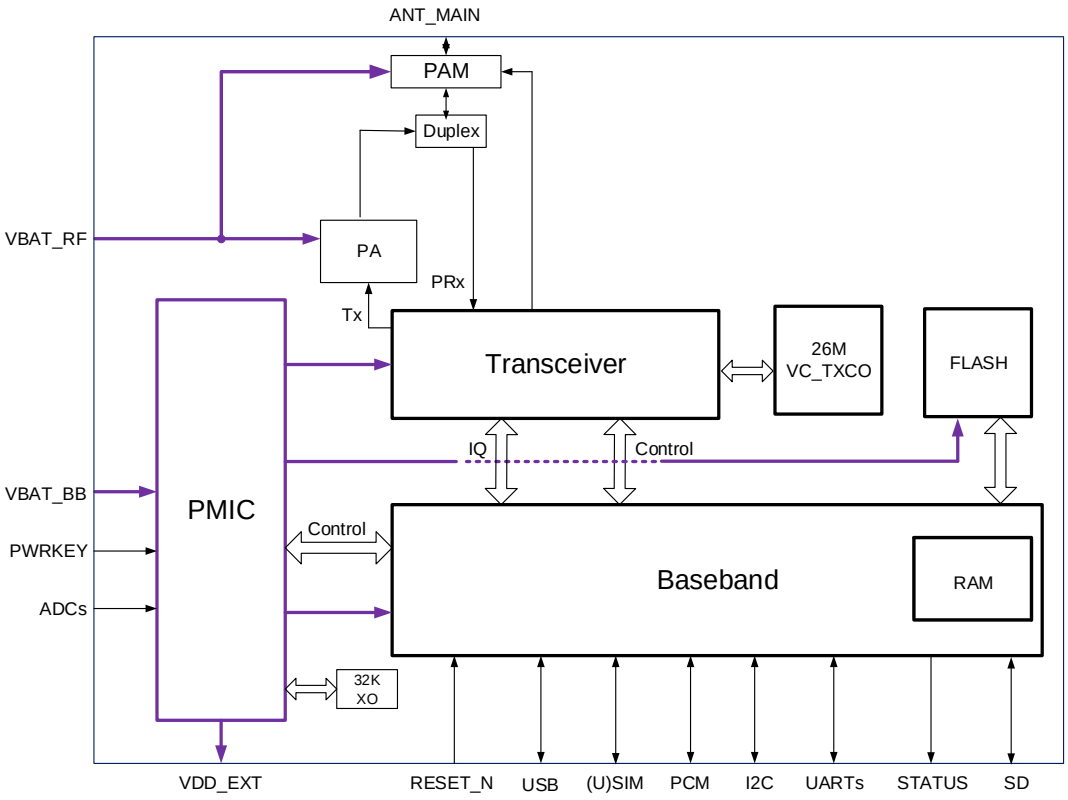


Figure 1: Functional Diagram

2.4. Evaluation Board

In order to help customers to develop applications with UC200T, Quectel provides an evaluation board (EVB), USB to RS-232 converter cable, earphone, antenna and other peripherals to control or test the module. For more details, please refer to ***document [4]***.

3 Application Interfaces

3.1. General Description

UC200T is equipped with 80 LCC pins and 64 LGA pins, which can be embedded into cellular application platforms. The following sections provide detailed descriptions of pins/interfaces listed below.

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SD card interface*
- ADC interfaces
- Status indication
- FORCE_USB_BOOT interface

NOTE

"*" means function of the SD card interface is under development.

3.2. Pin Assignment

The following figure shows the pin assignment of UC200T module.

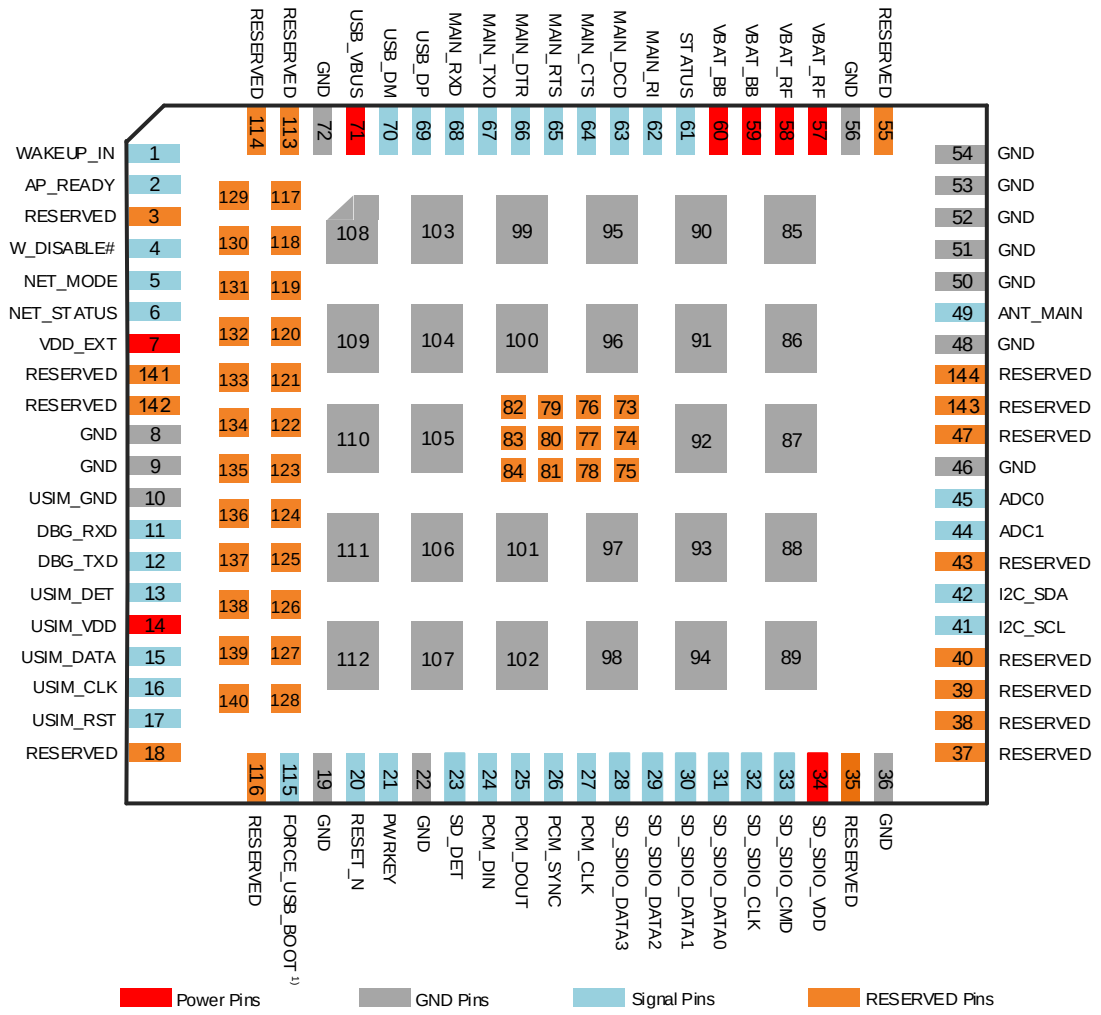


Figure 2: Pin Assignment (Top View)

NOTES

1. 1) means pin FORCE_USB_BOOT cannot be pulled up before startup.
2. If PCM_CLK, SD_SDIO_CLK, and I2C_SCL are not used, it is recommended to mount a 33pF capacitor close to each of the three pins to prevent interference from affecting RF's performance. Other unused pins and RESERVED pins should be kept open, and all GND pins should be connected to the ground.
3. GND pins 85~112 should be connected to ground. RESERVED pins 73~84 and 117~140 should not be used in schematics and PCB layout design, and these pins should be served as a keepout

area.
4. The function of the SD card interface is under development.

3.3. Pin Description

The following tables show the pin definition of UC200T module.

Table 4: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
IO	Bidirectional
OD	Open Drain
PI	Power Input
PO	Power Output

Table 5: Pin Description

Power Supply Input					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	Power supply for the module's baseband part	Vmax=4.5V Vmin=3.4V Vnorm=3.8V	It must be provided with sufficient current up to 0.8A.
VBAT_RF	57, 58	PI	Power supply for the module's RF part	Vmax=4.5V Vmin=3.4V Vnorm=3.8V	It must be provided with sufficient current up to 1.8A.
GND	8, 9, 19, 22, 36, 46, 48, 50~54,		Ground		

	56, 72, 85~112				
Power Supply Output					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VDD_EXT	7	PO	Provide 1.8V for external circuit	Vnorm=1.8V $I_O$max=50mA	Power supply for external GPIO's pull up circuits. If unused, keep it open.
Power on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESET_N	20	DI	Reset the module Active Low.	V_{IL}max=0.5V	If unused, keep it open.
PWRKEY	21	DI	Turn on/off the module	V_{IL}max=0.5V	VBAT power domain.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NET_MODE	5	DO	Indicate the module's network registration mode	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep it open.
NET_ STATUS	6	DO	Indicate the module's network activity status	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep it open.
STATUS	61	OD	Indicate the module's operation status		An external pull-up resistor is required. If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_DP	69	IO	USB differential data (+)		USB 2.0 compliant; 90Ω differential impedance; If unused, keep it open.
USB_DM	70	IO	USB differential data (-)		USB 2.0 compliant; 90Ω differential impedance. If unused, keep it

					open.
USB_VBUS	71	AI	USB connection detection	Vmax=5.25V Vmin=3.0V Vnorm=5.0V	Typical: 5.0V If unused, keep it open.
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	10		Dedicated ground for (U)SIM		A GND pin used to connect (U)SIM card connector.
USIM_DET	13	DI	(U)SIM card detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
USIM_VDD	14	PO	Power supply for (U)SIM card	Iomax=50mA **For 1.8V (U)SIM:** Vmax=1.9V Vmin=1.7V **For 3.0V (U)SIM:** Vmax=3.05V Vmin=2.7V	Either 1.8V or 3.0V (U)SIM card is supported and can be identified automatically by the module.
USIM_DATA	15	IO	(U)SIM data	**For 1.8V (U)SIM:** V_{IL}max=0.6V V_{IH}min=1.2V V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{IL}max=1.0V V_{IH}min=1.95V V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_CLK	16	DO	(U)SIM clock	**For 1.8V (U)SIM:** V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_RST	17	DO	(U)SIM reset	**For 1.8V (U)SIM:**	

				V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{OL}max=0.45V V_{OH}min=2.55V	
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RI	62	DO	Ring indication	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
MAIN_DCD	63	DO	Data carrier detection	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
MAIN_CTS	64	DO	Clear to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
MAIN_RTS	65	DI	Request to send	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
MAIN_DTR	66	DI	Data terminal ready	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
MAIN_TXD	67	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
MAIN_RXD	68	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	11	DI	Debug receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
DBG_TXD	12	DO	Debug transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it

					open.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC1	44	AI	General-purpose analog to digital converter	Voltage range: 0V to VBAT_BB	If unused, keep it open.
ADC0	45	AI	General-purpose analog to digital converter	Voltage range: 0V to VBAT_BB	If unused, keep it open.
PCM & I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_DIN	24	DI	PCM data input	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
PCM_DOUT	25	DO	PCM data output	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
PCM_SYNC	26	IO	PCM data frame synchronization	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it serves as an output signal. In slave mode, it serves as an input signal. If unused, keep it open.
PCM_CLK	27	IO	PCM clock	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it serves as an output signal. In slave mode, it serves as an input signal. If unused, it is recommended to mount a 33pF capacitor close to the pin.
I2C_SCL	41	OD	I2C serial clock for external codec		An external 1.8V pull-up resistor is required. If unused, it is

					recommended to mount a 33pF capacitor close to the pin.
I2C_SDA	42	OD	I2C serial data for external codec		An external 1.8V pull-up resistor is required. If unused, keep it open.
SD Card Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_DET	23	DI	SD card detect		1.8V/2.8V power domain. If unused, keep it open.
SD_SDIO_DATA3	28	IO	SD card SDIO data bit 3		1.8V/2.8V power domain. If unused, keep it open.
SD_SDIO_DATA2	29	IO	SD card SDIO data bit 2		1.8V/2.8V power domain. If unused, keep it open.
SD_SDIO_DATA1	30	IO	SD card SDIO data bit 1		1.8V/2.8V power domain. If unused, keep it open.
SD_SDIO_DATA0	31	IO	SD card SDIO data bit 0		1.8V/2.8V power domain. If unused, keep it open.
SD_SDIO_CLK	32	DO	SD card SDIO clock		1.8V/2.8V power domain. If unused, it is recommended to mount a 33pF capacitor close to the pin.
SD_SDIO_CMD	33	IO	SD card SDIO command		1.8V/2.8V power domain. If unused, keep it open.

SD_SDIO_VDD	34	PO	SD card SDIO power		1.8V/2.8V power domain. If unused, keep it open.
RF Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	49	IO	Main antenna		50Ω impedance
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN	1	DI	Wake up the module	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
AP_READY	2	DI	Application processor sleep state detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
W_DISABLE#	4	DI	Airplane mode control	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Pull-up by default. In the low voltage level, the module will enter airplane mode. If unused, keep it open.
FORCE_USB_BOOT	115	DI	Force USB boot	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Active high. It is recommended to reserve test points.
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	3, 18, 35 37~40, 43, 47, 55, 73~84, 113, 114, 116~144		Reserved		Keep these pins unconnected

NOTE

"*" means the function of SD card interface is under development.

3.4. Operating Modes

The following table briefly outlines the operating modes to be mentioned in the following sections.

Table 6: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	A network connection is ongoing. In this mode, the power consumption is decided by the network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** command can set the module to a minimum functionality mode without removing the power supply. In this case, both the RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** command or W_DISABLE# pin can set the module to airplane mode. In this case, the RF function will be invalid.	
Sleep Mode	In this mode, the current consumption of the module will be reduced to a minimal level. In this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	In this mode, the power management unit (PMU) shuts down the power supply, software goes inactive and the serial interfaces are not accessible. However, the VBAT_RF and VBAT_BB pins are still powered.	

3.5. Power Saving

3.5.1. Sleep Mode

UC200T is able to reduce its current consumption to an ultra-low value in the sleep mode. The following section describes the power saving procedure of UC200T module.

3.5.1.1. UART Application

If the host communicates with the module via UART interface, the following preconditions should be met to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive MAIN_DTR to a high level.

The following figure shows the connection between the module and the host.

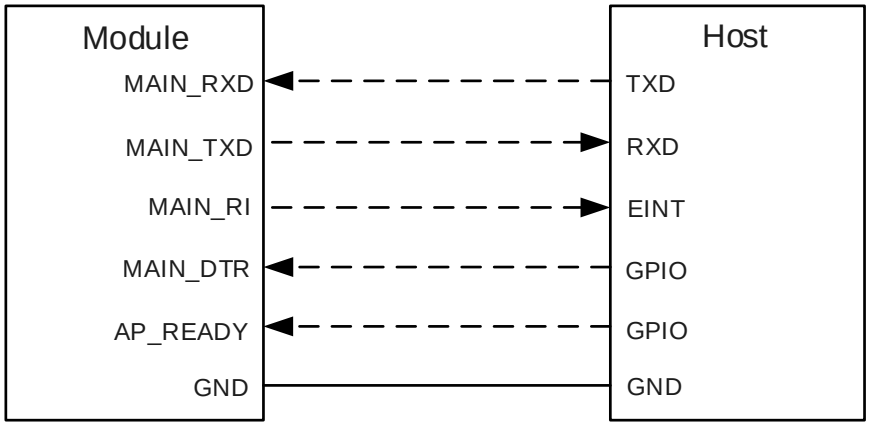


Figure 3: Sleep Mode Application via UART

- Driving MAIN_DTR to a low level by host will wake up the module.
- When UC200T has a URC to report, the URC will trigger the behavior of MAIN_RI pin. Please refer to ***Chapter 3.16*** for details about MAIN_RI behaviors.

3.5.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB Suspend/Resume and remote wakeup functions, the following three preconditions must be met to let the module enter sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the MAIN_DTR is kept at a high level or kept open.
- The host's USB bus, which is connected with the module's USB interface, enters the Suspend state.

The following figure shows the connection between the module and the host.

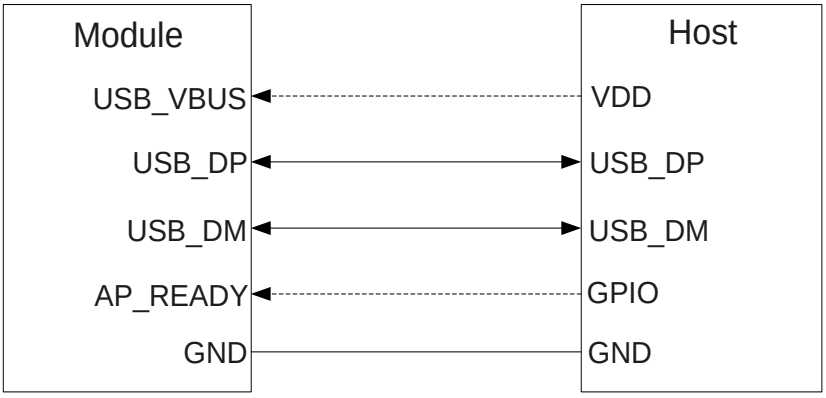


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to UC200T through USB will wake up the module.
- When UC200T has a URC to report, the module will send remote wakeup signals via USB bus so as to wake up the host.

3.5.1.3. USB Application with USB Suspend/Resume and MAIN_RI Wakeup Function

If the host supports USB Suspend/Resume, but does not support remote wake-up functions, the MAIN_RI signal is needed to wake up the host.

There are three preconditions to let the module enter the sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is kept at a high level or kept open.
- The host's USB bus, which is connected with the module's USB interface, enters the Suspend state.

The following figure shows the connection between the module and the host.

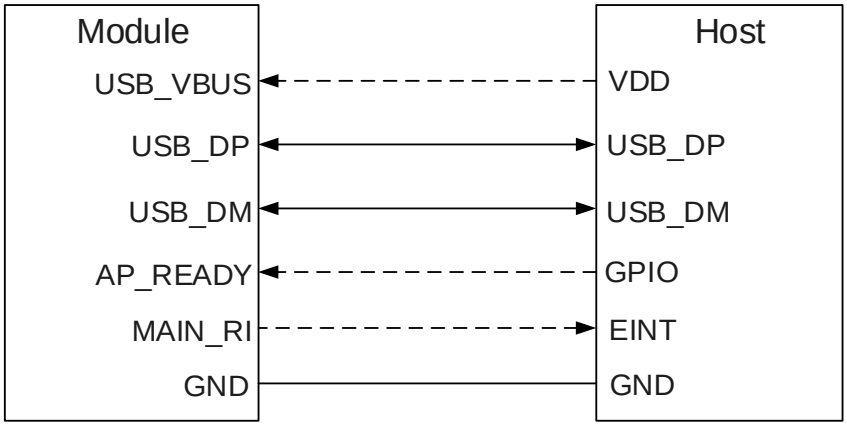


Figure 5: Sleep Mode Application with MAIN_RI

- Sending data to UC200T through USB will wake up the module.
- When UC200T has a URC to report, the URC will trigger the behavior of MAIN_RI pin.

3.5.1.4. USB Application without USB Suspend Function

If the host does not support USB Suspend function, please disconnect USB_VBUS with an additional control circuit to let the module enter sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the MAIN_DTR is held at a high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

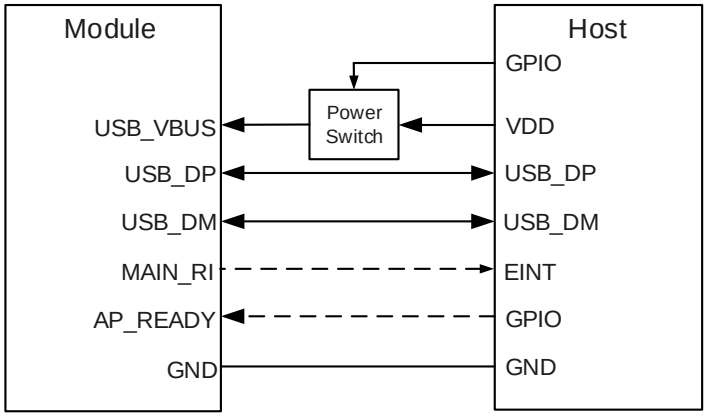


Figure 6: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

Please pay attention to the level match shown in the dotted line between the module and the host.

3.5.2. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default, and **AT+QCFG="airplanecontrol",1** can be used to enable the function. Driving it to a low level can make the module enter airplane mode.

Software:

AT+CFUN=<fun> provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode; both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

3.6. Power Supply

3.6.1. Power Supply Pins

UC200T provides four VBAT pins dedicated to connecting with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for the module's RF part
- Two VBAT_BB pins for the module's baseband part

The following table shows the details of power supply and GND pins.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	57, 58	Power supply for the module's RF part	3.4	3.8	4.5	V
VBAT_BB	59, 60	Power supply for the module's baseband part	3.4	3.8	4.5	V
GND	8, 9, 19, 22, 36, 46, 48, 50~54, 56, 72, 85~112	Ground	-	0	-	V

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.4V to 4.5V. Please make sure that the input voltage will never drop below 3.4V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G networks.

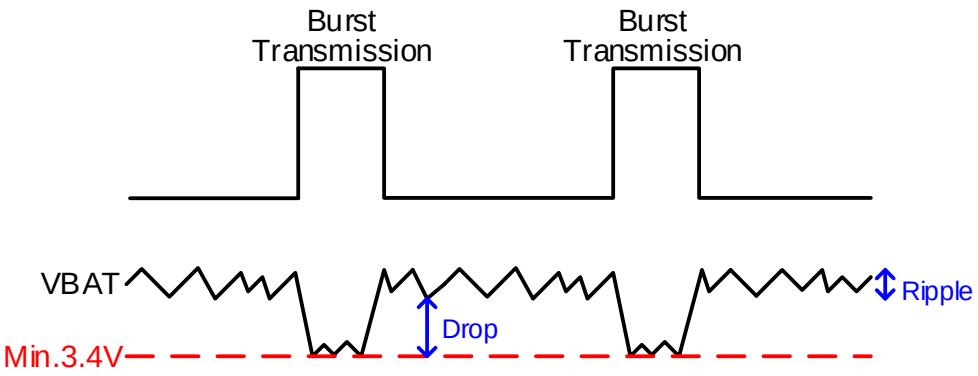


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array, and place these capacitors close to the VBAT_BB and VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with a star structure. The width of VBAT_BB trace should be no less than 1mm, and the width of VBAT_RF trace should be no less than 2mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to ensure the stability of power source, it is suggested that a TVS diode WS4.5D3HV of which reverse stand-off voltage is 4.7V and peak pulse power is up to 2550W should be used. The following figure shows the star structure of the power supply.

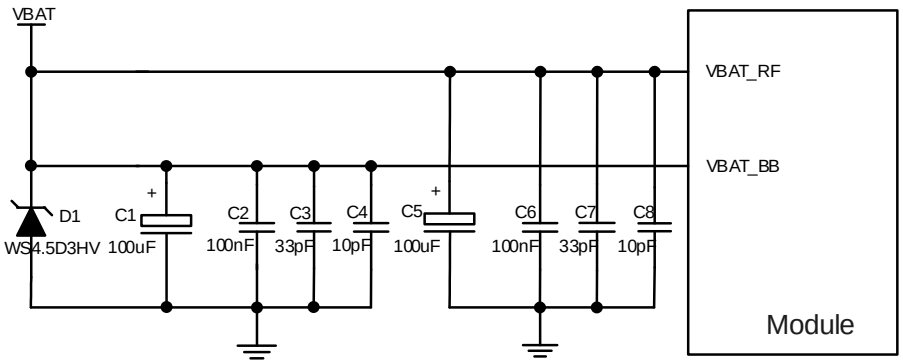


Figure 8: Star Structure of the Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 2.0A at least to the module. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.
The following figure shows a reference design for a +5V input power source. The typical output of the power supply is about 3.8V and the maximum load current is 3.0A.

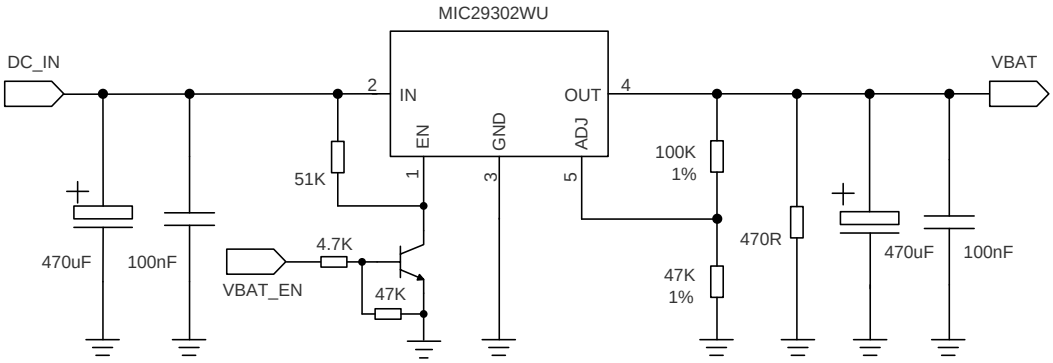


Figure 9: Reference Circuit of Power Supply

3.7. Power-on/off/Reset Scenarios

3.7.1. Turn on the Module Using the PWRKEY

The following table shows the pin definition of PWRKEY.

Table 8: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	VBAT power domain

When UC200T is in power-down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 500ms. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

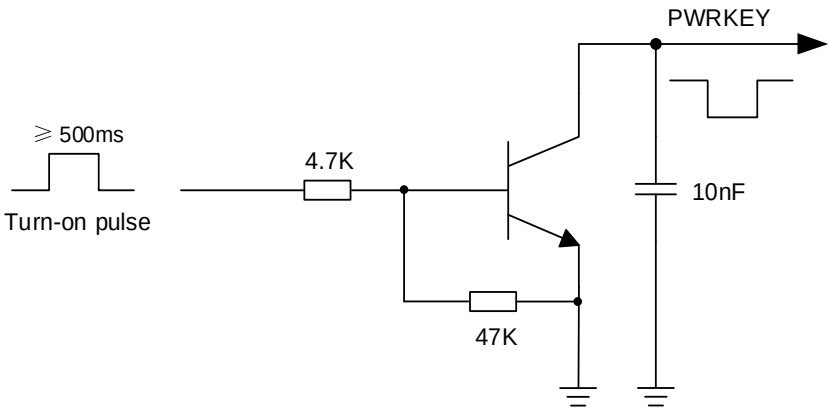


Figure 10: Reference Circuit of Turing on the Module Using Driving Circuit

The other way to control the PWRKEY is using a button directly. When pressing the key, an electrostatic strike may generate from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

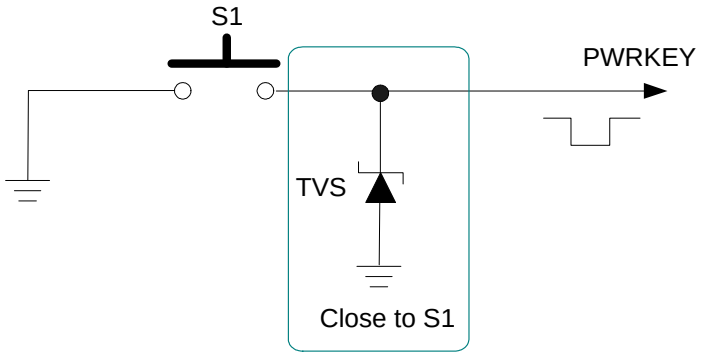


Figure 11: Reference Circuit of Turing on the Module Using Keystroke

The timing of turning on the module is illustrated in the following figure.

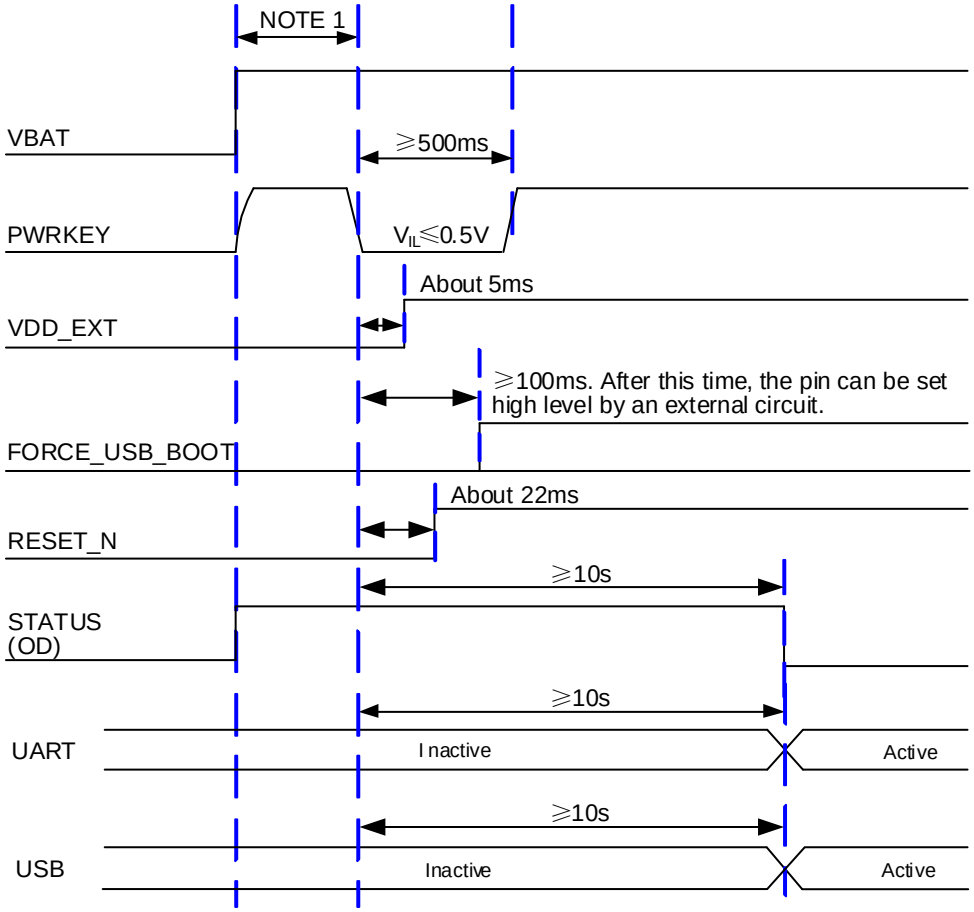


Figure 12: Timing of Turning on the Module

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 30ms.
2. PWRKEY can be pulled down directly to GND with a recommended 4.7kΩ resistor if the module needs to be powered on automatically and shutdown is not needed.

3.7.2. Turn off the Module

The following procedures can be used to turn off the module:

- Using the PWRKEY pin.
- Using **AT+QPOWD** command.

3.7.2.1. Turn off the Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low-level voltage for at least 650ms, the module will execute power-down procedure after the PWRKEY is released. The timing of turning off the module is illustrated in the following figure.

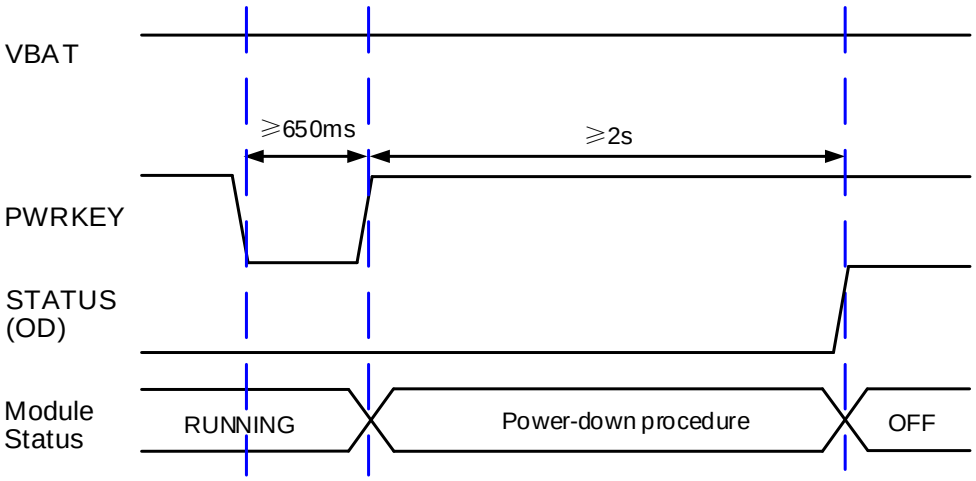


Figure 13: Timing of Turning off the Module

3.7.2.2. Turn off Module Using AT Command

It is also a safe way to use **AT+QPOWD** command to turn off the module, which is similar to the procedure of turning off the module via PWRKEY pin.

Please refer to ***document [2]*** for details about **AT+QPOWD** command.

NOTES

1. In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.
2. When turning off the module with the AT command, please keep PWRKEY at a high level after the execution of the command. Otherwise, the module will turn itself back on after being shut down.

3.7.3. Reset the Module

The RESET_N pin can be used to reset the module. The module can be reset by pulling the RESET_N pin low for at least 300ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended that the traces between the RESET_N pin and customers' device should be as short as possible and must be encircled by ground traces.

Table 9: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module. Active low.	1.8V power domain. If unused, keep it open.

The recommended circuit is similar to the PWRKEY control circuit. An open-drain/collector driver or button can be used to control the RESET_N.

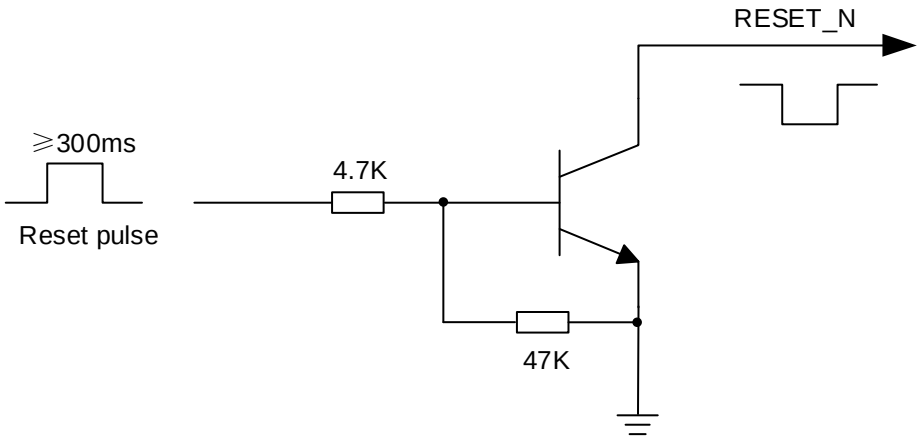


Figure 14: Reference Circuit of Resetting the Module by Using Driving Circuit

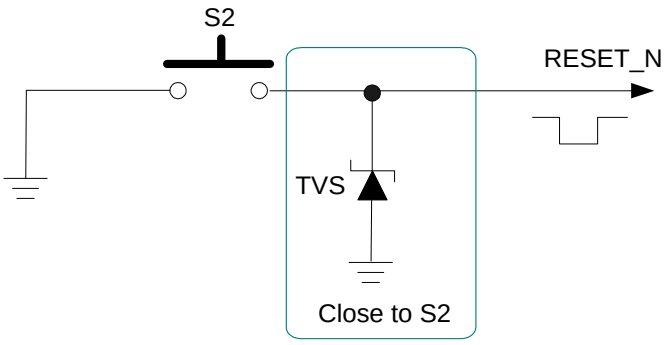


Figure 15: Reference Circuit of Resetting the Module by Using Button

The timing of resetting module is illustrated in the following figure.

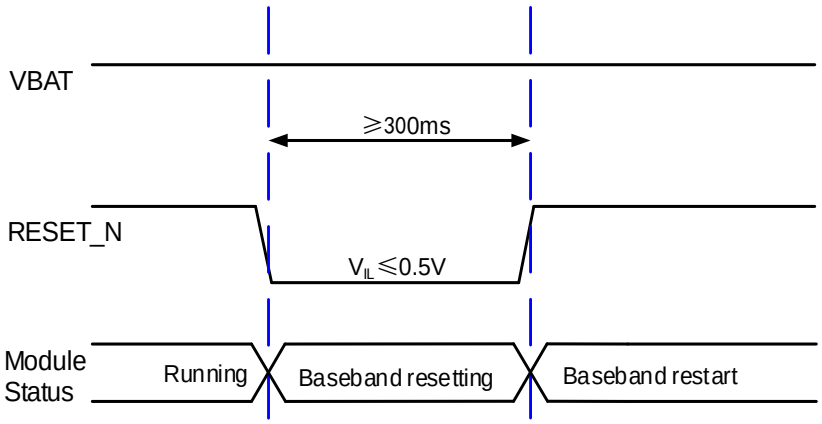


Figure 16: Timing of Resetting Module

NOTES

1. Please make sure that there is no large capacitance with the max value exceeding 10nF on PWRKEY and RESET_N pins.
2. RESET_N only resets the internal baseband chip of the module and does not reset the power management chip.
3. It is recommended to use RESET_N only when fail to turn off the module by **AT+QPOWD** command or PWRKEY pin.

3.8. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 SIM interface requirements. Both 1.8V and 3.0V (U)SIM cards are supported.

Table 10: Pin Definition of the (U)SIM Card Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_GND	10		Dedicated ground for (U)SIM	
USIM_DET	13	DI	(U)SIM card detection	1.8V power domain. If unused, keep it open.
USIM_VDD	14	PO	Power supply for (U)SIM card	Either 1.8V or 3.0V (U)SIM card is supported and can be identified automatically by the module.

USIM_DATA	15	IO	(U)SIM data
USIM_CLK	16	DO	(U)SIM clock
USIM_RST	17	DO	(U)SIM reset

UC200T supports (U)SIM card hot-plug via the USIM_DET pin. The function supports low-level and high-level detections. By default, it is disabled and can be configured via **AT+QSIMDET**. Please refer to ***document [2]*** for details about the command.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

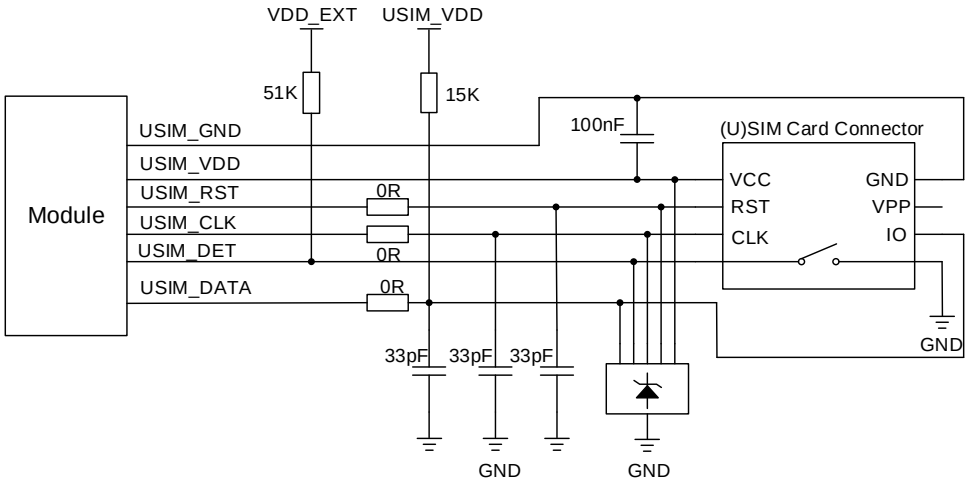


Figure 17: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

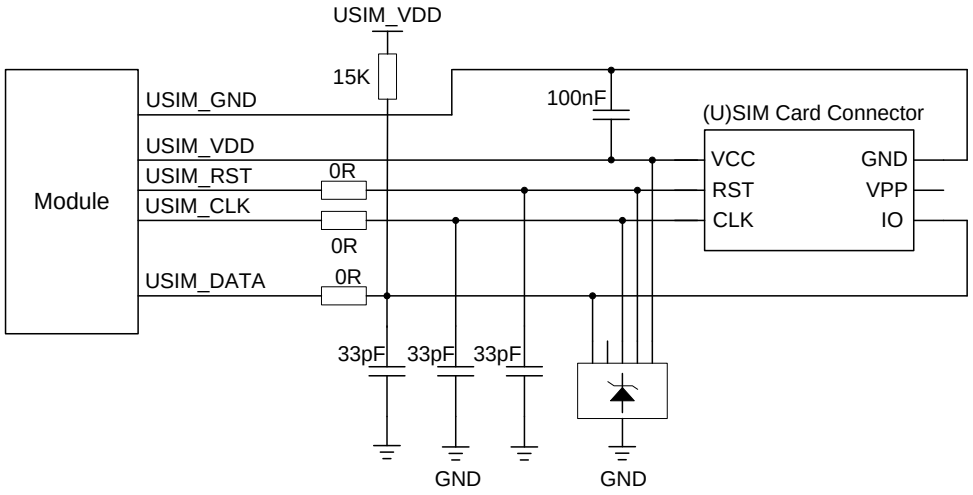


Figure 18: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in customers' applications, please follow the criteria below in (U)SIM circuit design:

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length less than 200mm as far as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential. If the ground is complete on customers' PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with the surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 15pF. The 0Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33pF capacitors are used for filtering interference of GSM900MHz. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

3.9. USB Interface

UC200T provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports full-speed (12Mbps) and high-speed (480Mbps) modes. The USB interface can only serve as a slave device and is used for AT command communication, data transmission, software debugging and firmware upgrade. The following table shows the pin definition of USB interface.

Table 11: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	69	IO	USB differential data (+)	90Ω differential impedance
USB_DM	70	IO	USB differential data (-)	90Ω differential impedance
USB_VBUS	71	AI	USB connection detection	Typical 5.0V
GND	72		Ground	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

It is recommended to reserve the USB interface for firmware upgrade on customers' designs. The following figure shows a reference circuit of the USB interface.

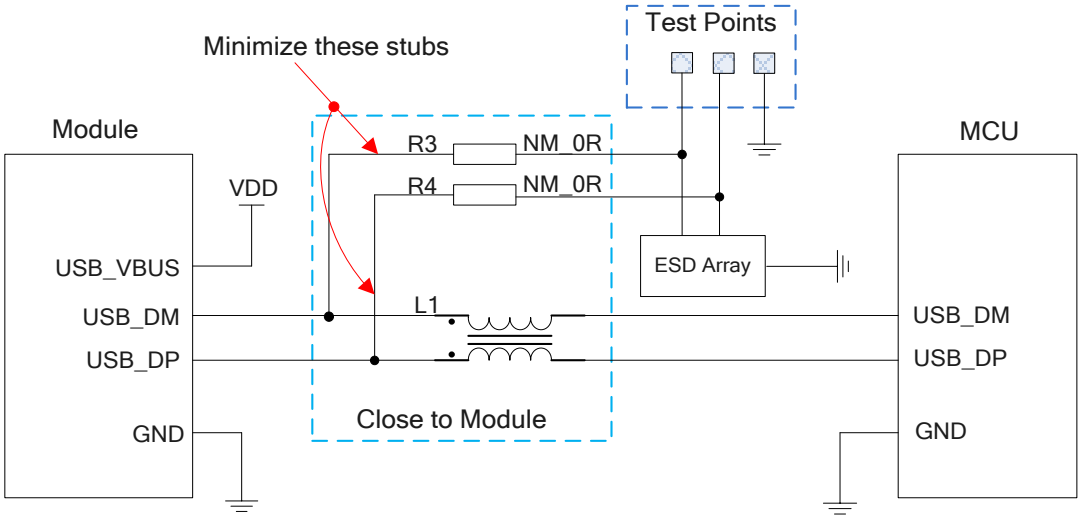


Figure 19: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission. Meanwhile, the 0Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of the USB data line signal, L1, R3 and R4 components must be placed close to the module, and also resistors R3 and R4 should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be followed when designing the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Please pay attention to the selection of the ESD component on the USB data line. Its parasitic capacitance should not exceed 2pF and should be placed as close as possible to the USB interface.

3.10. UART Interfaces

The module provides two UART interfaces: the main UART interface and the debug UART interface. The features of these interfaces are shown below.

- The main UART interface supports 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps, 460800bps, 921600bps and 1Mbps baud rates, and the default is 115200bps. This interface is used for data transmission and AT command communication.
- The debug UART interface supports 115200bps baud rate. It is used for outputting partial logs.

The following tables show the pin definition of main UART interface.

Table 12: Pin Definition of the Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RI	62	DO	Ring indication	1.8V power domain. If unused, keep open.
MAIN_DCD	63	DO	Data carrier detection	
MAIN_CTS	64	DO	DTE clear to send	
MAIN_RTS	65	DI	DTE request to send	
MAIN_DTR	66	DI	Data terminal ready	
MAIN_TXD	67	DO	Transmit data	
MAIN_RXD	68	DI	Receive data	

Table 13: Pin Definition of the Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	11	DI	Debug receive data	1.8V power domain.
DBG_TXD	12	DO	Debug transmit data	

The logic levels are described in the following table.

Table 14: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides a 1.8V UART interface. A level translator should be used if the application is equipped with a 3.3V UART interface. A level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design.

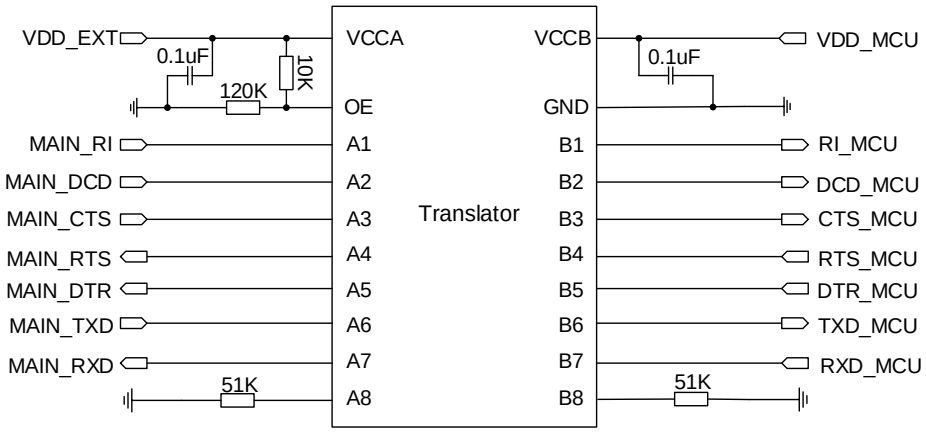


Figure 20: Reference Circuit with a Level Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown below. For the design of circuits in dotted lines, please refer to that of the circuits in solid lines, but please pay attention to the direction of connection.

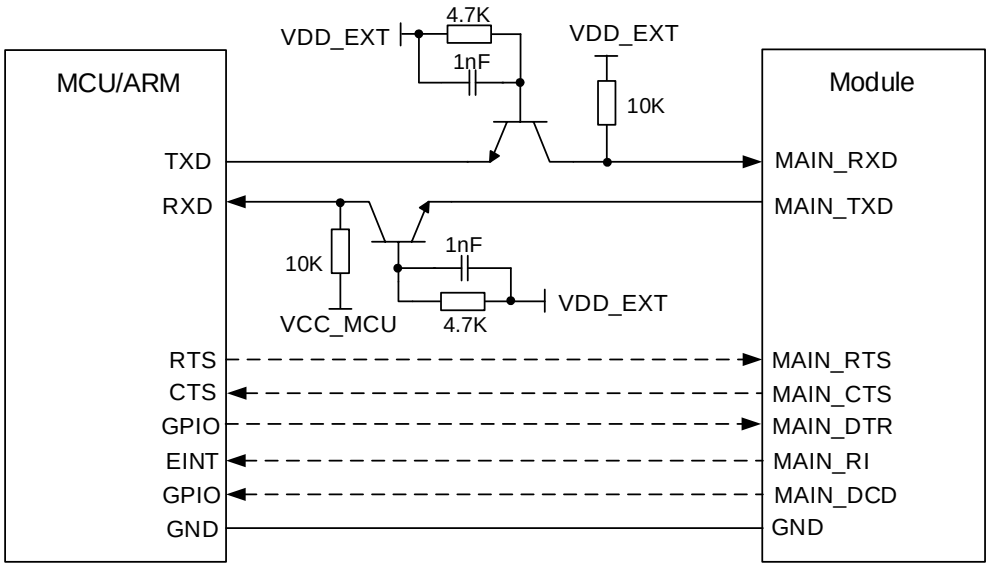


Figure 21: Reference Circuit with a Transistor Circuit

NOTE

The transistor circuit solution is not suitable for applications with baud rates exceeding 460Kbps.

3.11. PCM and I2C Interfaces

UC200T provides one Pulse Code Modulation (PCM) digital interface for audio design, which supports the primary mode (short frame synchronization) and UC200T works as both master and slave.

UC200T works as a master device pertaining to I2C interface.

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256kHz, 512kHz, 1024kHz or 2048kHz PCM_CLK at 8kHz PCM_SYNC, and also supports 4096kHz PCM_CLK at 16kHz PCM_SYNC.

UC200T supports 16-bit linear data format. The following figure shows the primary mode's timing relationship with 8kHz PCM_SYNC and 2048kHz PCM_CLK.

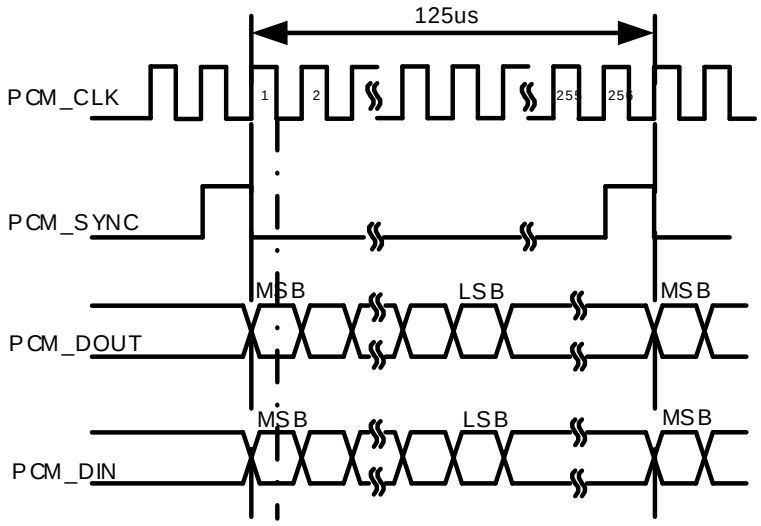


Figure 22: Primary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 15: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	24	DI	PCM data input	1.8V power domain If unused, keep it open
PCM_DOUT	25	DO	PCM data output	1.8V power domain If unused, keep it open
PCM_SYNC	26	IO	PCM data frame synchronization	1.8V power domain. In master mode, it serves as an output signal. In slave mode, it is used as an input signal. If unused, keep it open.
PCM_CLK	27	IO	PCM clock	1.8V power domain In master mode, it serves as an output signal. In slave mode, it is used as an input signal. If unused, it is recommended to mount a 33pF capacitor close to the pin.
I2C_SCL	41	OD	I2C serial clock for an	An external 1.8V pull-up resistor

			external codec	is required. If unused, it is recommended to mount a 33pF capacitor close to the pin.
I2C_SDA	42	OD	I2C serial data for an external codec	An external 1.8V pull-up resistor is required. If unused, keep it open.

Clock and mode can be configured by AT command, and the default configuration is short frame synchronization format with 2048kHz PCM_CLK and 8kHz PCM_SYNC.

The following figure shows a reference design of a PCM interface with external codec IC.

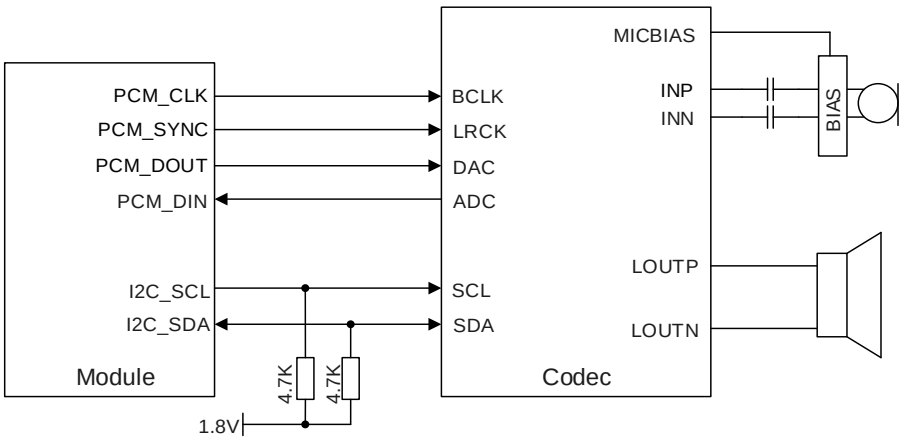


Figure 23: Reference Circuit of PCM Application with Audio Codec

NOTE

It is recommended to reserve an RC (R=22Ω, C=22pF) circuit on the PCM lines, especially for PCM_CLK.

3.12. SD Card Interface*

UC200T provides an SD card interface, which complies with SD 3.0 specification.

The following table shows the pin definition of the SD card interface.

Table 16: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_DET	23	DI	SD card detect	1.8V/2.8V power domain. If unused, keep it open.
SD_SDIO_DATA3	28	IO	SD card SDIO data bit 3	1.8V/2.8V power domain. If unused, keep it open.
SD_SDIO_DATA2	29	IO	SD card SDIO data bit 2	1.8V/2.8V power domain. If unused, keep it open.
SD_SDIO_DATA1	30	IO	SD card SDIO data bit 1	1.8V/2.8V power domain. If unused, keep it open.
SD_SDIO_DATA0	31	IO	SD card SDIO data bit 0	1.8V/2.8V power domain. If unused, keep it open.
SD_SDIO_CLK	32	DO	SD card SDIO clock	1.8V/2.8V power domain. If unused, it is recommended to mount a 33pF capacitor close to the pin.
SD_SDIO_CMD	33	IO	SD card SDIO command	1.8V/2.8V power domain. If unused, keep it open.
SD_SDIO_VDD	34	PO	SD card SDIO power	1.8V/2.8V power domain. If unused, keep it open.

The following figure shows a reference design of the SD card interface.

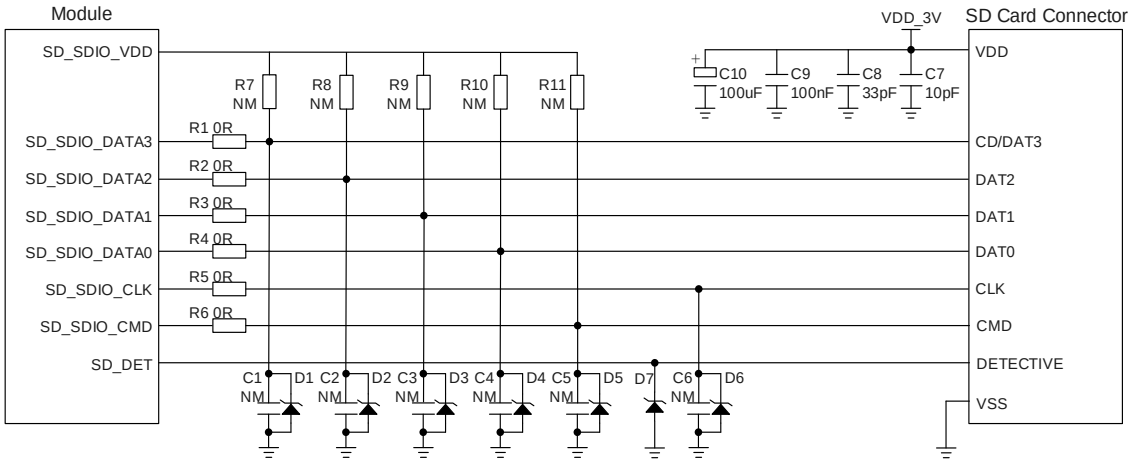


Figure 24: Reference Circuit of SD Card Interface

In SD card interface design, in order to ensure good communication performance with SD card, the following design principles should be complied with:

‘

- he voltage range of SD card power supply VDD_3V is 2.7V~3.6V and a sufficient current up to 0.8A should be provided. As the maximum output current of SD_SDIO_VDD is 50mA which can only be used for SDIO pull-up resistors, an external power supply is needed for SD card.
- To avoid jitter of bus, resistors R7~R11 are needed to pull up the SDIO to SD_SDIO_VDD. Value of these resistors is among 10kΩ~100kΩ and the recommended value is 100kΩ. SD_SDIO_VDD should be used as the pull-up power.
- In order to adjust signal quality, it is recommended to add 0Ω resistors R1~R6 in series between the module and the SD card. The bypass capacitors C1~C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- In order to offer good ESD protection, it is recommended to add a TVS diode on SD card pins near the SD card connector with junction capacitance less than 15pF.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc .
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50Ω (±10%).
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 15pF.
- It is recommended to keep the traces of SD_SDIO_CLK, SD_SDIO_DATA[0:3] and SD_SDIO_CMD with equal length (the difference among them is less than 1mm) and the total routing length needs to be less than 50mm.

NOTE

"*" means the function of the SD card interface is under development.

3.13. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces. **AT+QADC=0** can be used to read the voltage value on ADC0 pin. **AT+QADC=1** can be used to read the voltage value on ADC1 pin. For more details about these AT commands, please refer to the ***document [2]***.

In order to improve the accuracy of ADC, the traces of ADC interfaces should be encircled by ground traces.

Table 17: Pin Definition of the ADC Interfaces

Pin Name	Pin No.	Description
ADC1	44	General-purpose analog to digital converter
ADC0	45	General-purpose analog to digital converter

The following table describes the characteristic of the ADC function.

Table 18: Characteristic of the ADC

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0		VBAT_BB	V
ADC1 Voltage Range	0		VBAT_BB	V
ADC Resolution		12		bits

NOTE

It is recommended to use a resistor divider circuit for ADC application.

3.14. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two pins which are NET_MODE and NET_STATUS for network status indication. The following tables describe pin definition and logic level changes in different network status.

Table 19: Pin Definition of Network Connection Status/Activity Indication

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	5	DO	Indicate the module's network registration mode.	1.8V power domain. If unused, keep it open.
NET_STATUS	6	DO	Indicate the module's network activity status.	1.8V power domain. If unused, keep it open.

Table 20: Working State of the Network Connection Status/Activity Indication

Pin Name	Logic Level Changes	Network Status
NET_MODE	Always high	Registered on UMTS network
	Always low	Others
NET_STATUS	Flicker slowly (200ms high/1800ms low)	Network searching
	Flicker slowly (1800ms high/200ms low)	Idle
	Flicker quickly (125ms high/125ms low)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

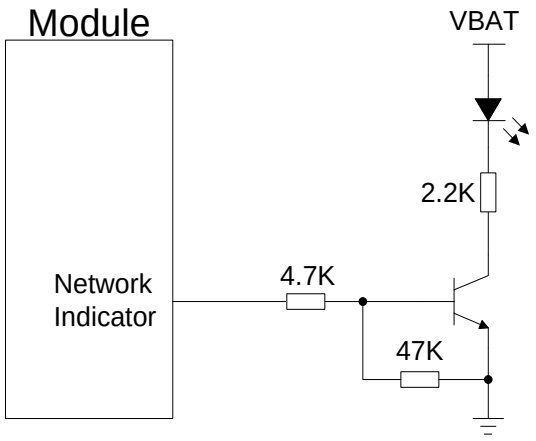


Figure 25: Reference Circuit of the Network Status Indication

3.15. STATUS

The STATUS pin is an open drain output for the module's operation status indication. It can be connected to a GPIO of DTE with a pulled-up resistor, or as an LED indication circuit as below. When the module is turned on normally, the STATUS will present the low state. Otherwise, the STATUS will present high-impedance state.

Table 21: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	OD	Indicate the module's operation status	An external pull-up resistor is required. If unused, keep it open.

The following figure shows different circuit designs of STATUS, and customers can choose either one according to the application demands.

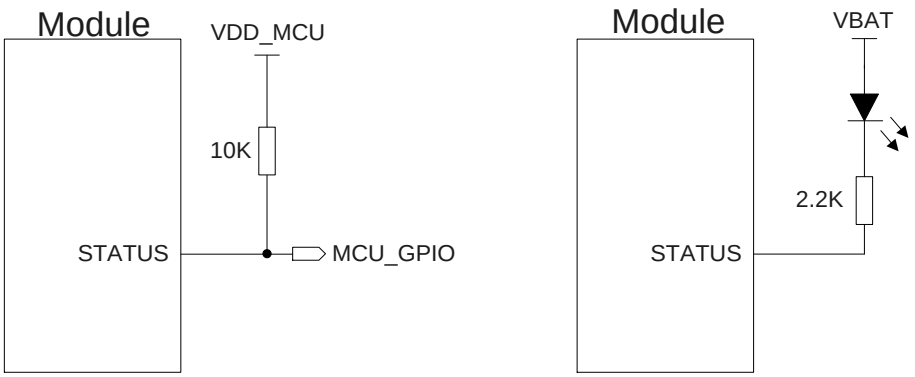


Figure 26: Reference Circuits of STATUS

NOTE

The status pin cannot be used as an indication of module shutdown status when VBAT is removed.

3.16. Behaviors of the MAIN_RI

AT+QCFG="risignaltype","physical" command can be used to configure MAIN_RI behaviors.

No matter on which port a URC is presented, the URC will trigger behaviors of the MAIN_RI pin.

NOTE

The URC can be outputted from the UART port, USB AT port and USB modem port, which can be set by **AT+QURCCFG**. The default port is USB AT port.

In addition, the MAIN_RI behavior can be configured flexibly. The default behavior of the MAIN_RI is shown below.

Table 22: Behaviors of the MAIN_RI

State	Response
Idle	MAIN_RI keeps at a high level
URC	MAIN_RI outputs 120ms low pulse when a new URC is returned

The MAIN_RI behavior can be changed via **AT+QCFG="urc/ri/ring"** *. Please refer to ***document [2]*** for details.

NOTE

"*" means under development.

3.17. FORCE_USB_BOOT Interface

UC200T provides a FORCE_USB_BOOT pin. Customers can pull up FORCE_USB_BOOT to 1.8V before VDD_EXT is powered up, and the module will enter emergency download mode when it is powered on. In this mode, the module supports firmware upgrade over a USB interface.

Table 23: Pin Definition of FORCE_USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
FORCE_USB_BOOT	115	DI	Force the module to enter emergency download mode	1.8V power domain. Active high. It is recommended to reserve test points.

The following figure shows a reference circuit of FORCE_USB_BOOT interface.

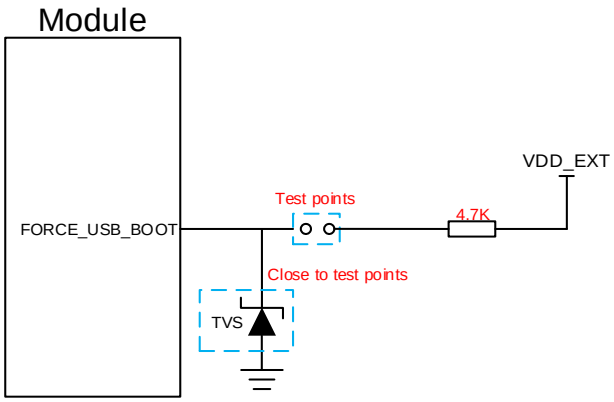


Figure 27: Reference Circuit of FORCE_USB_BOOT Interface

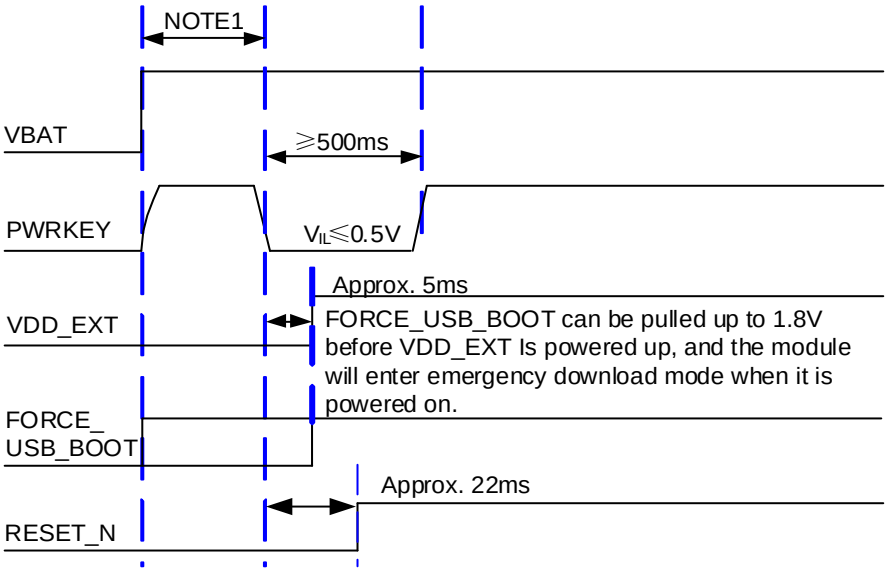


Figure 28: Timing Sequence for Entering Emergency Download Mode

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30ms.
2. When using MCU to control module to enter the forced emergency download mode, please follow the above timing sequence. It is not recommended to pull up FORCE_USB_BOOT to 1.8V before powering up the VBAT. Directly connect the two test points as shown in ***Figure 27*** will

manually	force the module to enter download mode.

4 Antenna Interface

UC200T provides one main antenna interface with an impedance of 50Ω.

4.1. Main Antenna Interface

4.1.1. Pin Definition

The pin definition of the main antenna interface is shown below.

Table 24: Pin Definition of the RF Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	49	IO	Main antenna	50Ω impedance

4.1.2. Operating Frequency

Table 25: UC200T-EM Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
EGSM900	880~915	925~960	MHz
DCS1800	1710~1785	1805~1880	MHz
WCDMA B1	1920~1980	2110~2170	MHz
WCDMA B8	880~915	925~960	MHz

Table 25: UC200T-GL Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
GSM850	824~850	869~894	MHz
EGSM900	880~915	925~960	MHz
DCS1800	1710~1785	1805~1880	MHz
PCS1900	1850~1910	1930~1990	MHz
WCDMA B1	1920~1980	2110~2170	MHz
WCDMA B2	1852~1908	1932~1988	MHz
WCDMA B5	826~847	871~892	MHz
WCDMA B6	832~838	877~883	MHz
WCDMA B8	880~915	925~960	MHz

4.1.3. Reference Design of RF Antenna Interface

A reference design of ANT_MAIN antenna pin is shown as below. It should reserve a π-type matching circuit for better RF performance. The capacitors are not mounted by default.

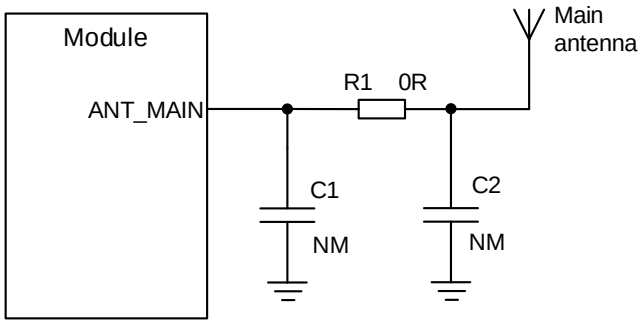


Figure 29: Reference Circuit of RF Antenna Interface

NOTE

Place the π-type matching components (R1/C1/C2 and R2/C3/C4) as close to the antenna as possible.

4.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following figures are reference designs of microstrip line or coplanar waveguide with different PCB structures.

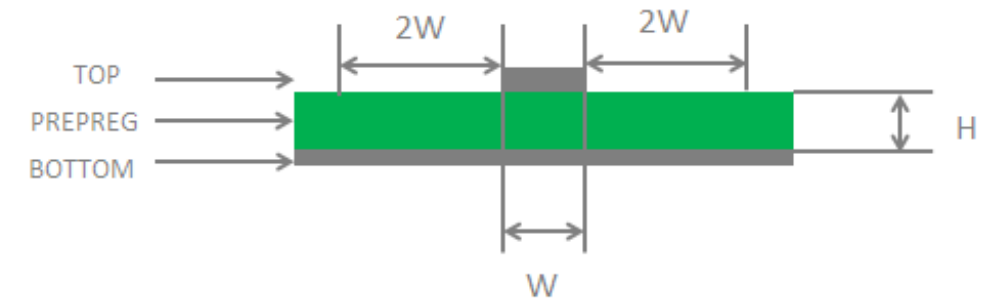


Figure 30: Microstrip Design on a 2-layer PCB

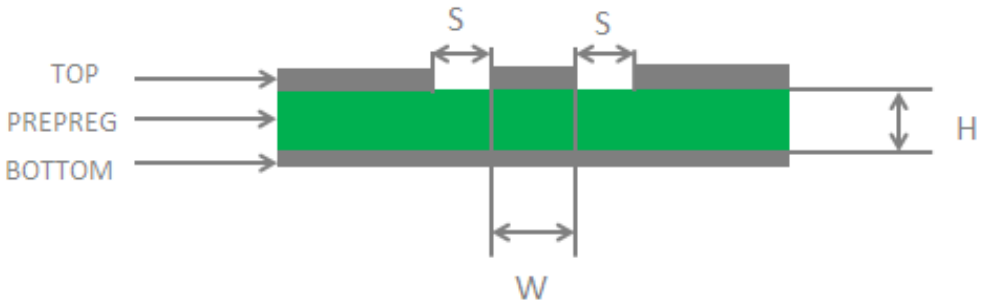


Figure 31: Coplanar Waveguide Design on a 2-layer PCB

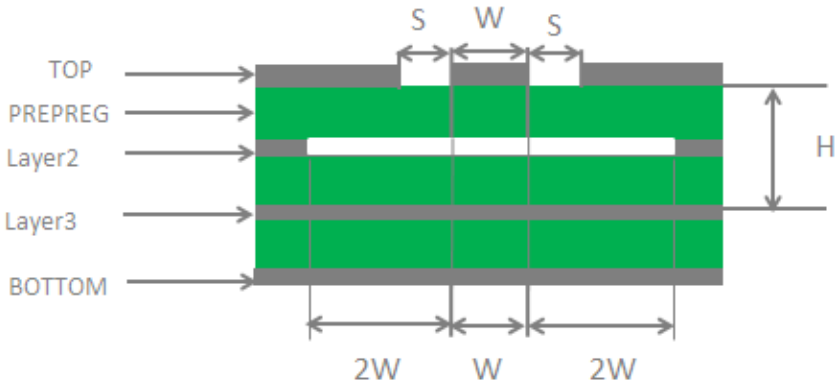


Figure 32: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

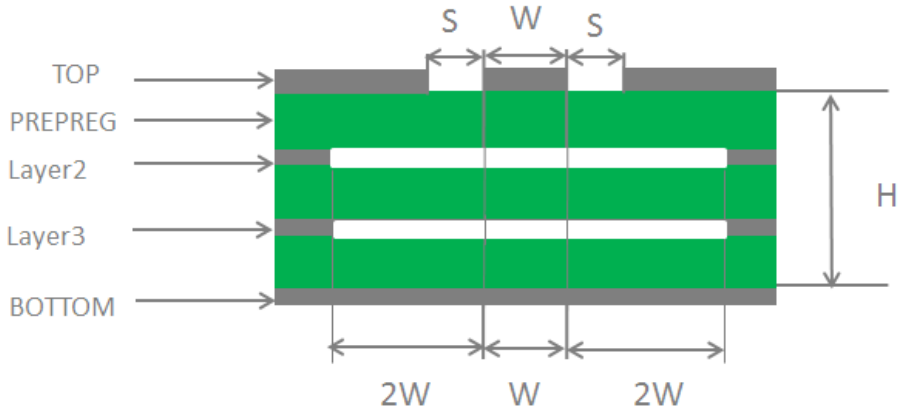


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times as wide as RF signal traces (2 × W).

For more details about the RF layout, please refer to the ***document [3]***.

4.2. Antenna Installation

4.2.1. Antenna Requirement

The following table shows the requirements on the main antenna.

Table 26: Antenna Requirements

Type	Requirements
GSM/WCDMA	VSWR: ≤2 Efficiency: >30% Max input power: 50W Input impedance: 50Ω Cable insertion loss: <1dB (GSM850/EGSM900, WCDMA B5/B6/B8) Cable insertion loss <1.5dB (DCS1800/PCS1900, WCDMA B1/B2)

4.2.2. Recommended RF Connector for Antenna Installation

If an RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

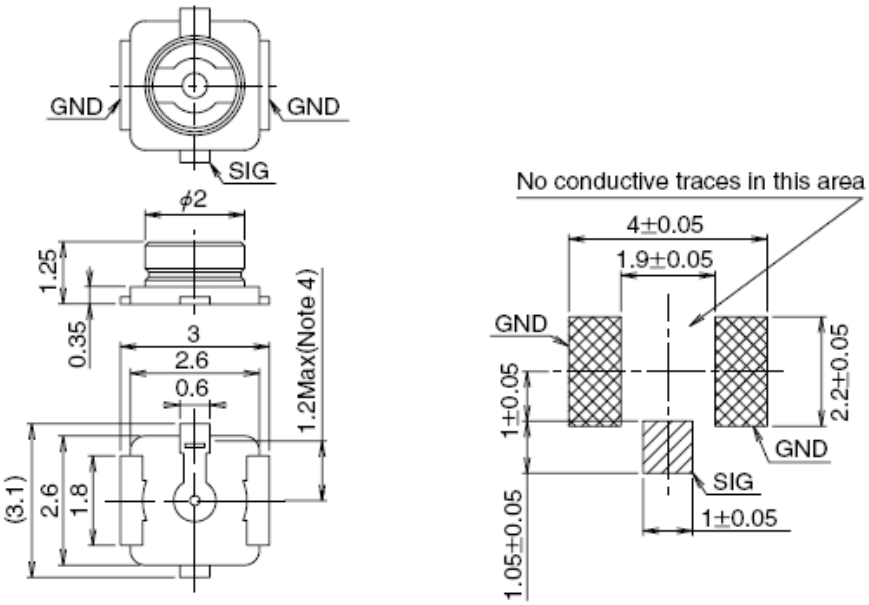


Figure 34: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

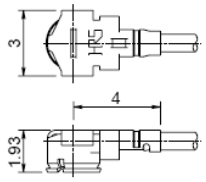
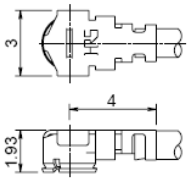
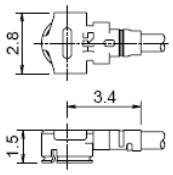
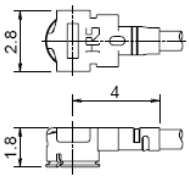
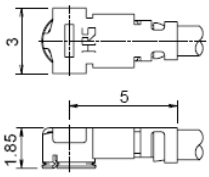
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 35: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connectors.

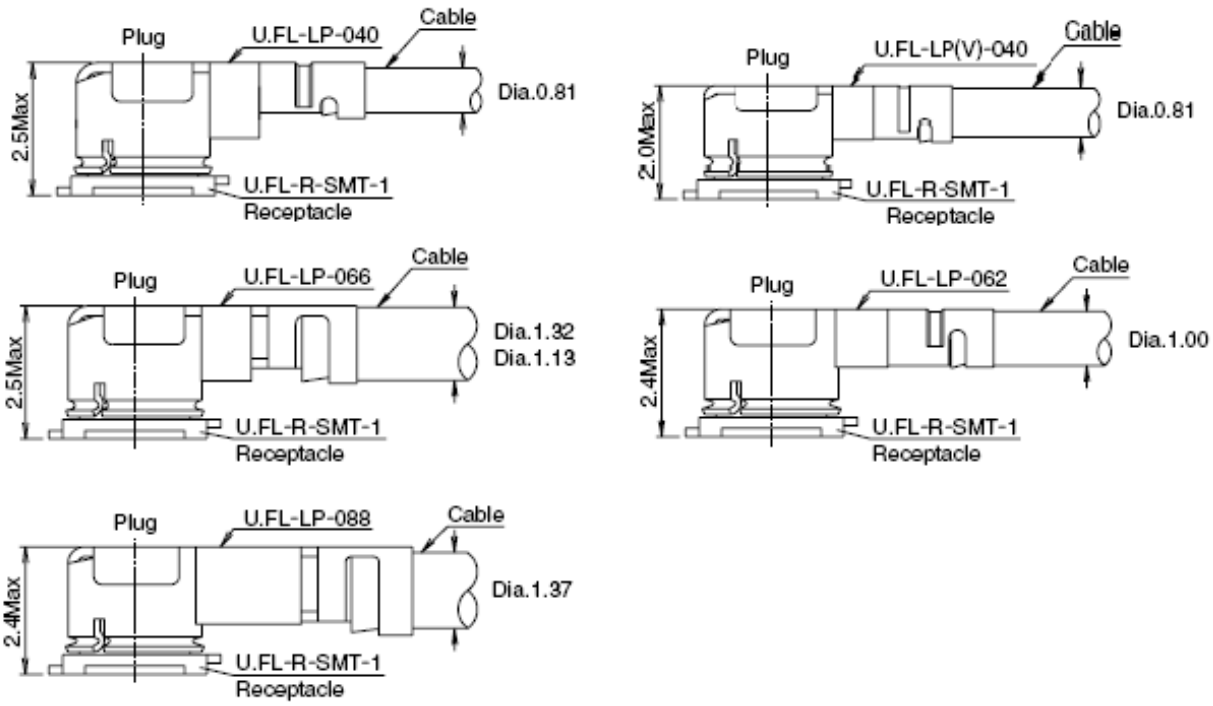


Figure 36: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://hirose.com.

5 Electrical, Reliability and Radio Characteristics

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 27: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	1.8	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V

5.2. Power Supply Ratings

Table 28: The Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.4	3.8	4.5	V
	Voltage drop during burst transmission	Maximum power control level on GSM850/EGSM900.			400	mV
I_{VBAT}	Peak supply current (during each transmission slot)	Maximum power control level on GSM850/EGSM900.		1.8	2.0	A
USB_VBUS	USB connection detection		3.0	5.0	5.25	V

5.3. Operation and Storage Temperatures

The operation and storage temperatures are listed in the following table.

Table 29: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range [1)]	-35	+25	+75	ºC
Extended Operation Range [2)]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1)] Within the operation temperature range, the module is 3GPP compliant.
2. [2)] Within the extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce their value and exceed the specified tolerances. When the temperature returns to the

normal operating temperature levels, the module will meet 3GPP specifications again.

5.4. Current Consumption

Table 30: UC200T-EM Current Consumption

Parameter	Description	Condition	Typical	Unit
I_{VBAT}	Power off	Module power off	14	uA
	Sleep mode	**AT+CFUN=0** (USB disconnected)	1.00	mA
		EGSM900 @DRX=2 (USB disconnected)	2.78	mA
		EGSM900 @DRX=5 (USB disconnected)	1.80	mA
		EGSM900 @DRX=5 (USB suspend)	1.92	mA
		EGSM900 @DRX=9 (USB disconnected)	1.44	mA
		DCS1800 @DRX=2 (USB disconnected)	2.70	mA
		DCS1800 @DRX=5 (USB disconnected)	1.76	mA
		DCS1800 @DRX=5 (USB suspend)	1.76	mA
		DCS1800 @DRX=9 (USB disconnected)	1.45	mA
		WCDMA @PF=64 (USB disconnected)	4.24	mA
		WCDMA @PF=64 (USB suspend)	4.38	mA
		WCDMA @PF=128 (USB disconnected)	2.60	mA
		WCDMA @PF=256 (USB disconnected)	1.95	mA
		WCDMA @ PF=512 (USB disconnected)	1.50	mA
	Idle mode	EGSM900 @DRX=5 (USB disconnected)	33.00	mA

		EGSM900 @DRX=5 (USB connected)	33.16	mA
		WCDMA @PF=64 (USB disconnected)	34.82	mA
		WCDMA @PF=64 (USB connected)	34.95	mA
	GPRS data transfer	EGSM900 4DL/1UL @32.58dBm	262.3	mA
		EGSM900 3DL/2UL @32.28dBm	432.5	mA
		EGSM900 2DL/3UL @30.8dBm	520.9	mA
		EGSM900 1DL/4UL @28.78dBm	543.5	mA
		DCS1800 4DL/1UL @29.28dBm	208.5	mA
		DCS1800 3DL/2UL @29.1dBm	320.8	mA
		DCS1800 2DL/3UL @27.51dBm	380.5	mA
		DCS1800 1DL/4UL @25.47dBm	400.8	mA
	EDGE data transfer	EGSM900 4DL/1UL @26.78dBm	202.6	mA
		EGSM900 3DL/2UL @26.57dBm	315.8	mA
		EGSM900 2DL/3UL @24.99dBm	412.7	mA
		EGSM900 1DL/4UL @22.12dBm	513.2	mA
		DCS1800 4DL/1UL @25.13dBm	191.6	mA
		DCS1800 3DL/2UL @25.13dBm	290.9	mA
		DCS1800 2DL/3UL @23.54dBm	371.3	mA
		DCS1800 1DL/4UL @21.45dBm	443.3	mA
	WCDMA data transfer	WCDMA B1 HSDPA @23.2dBm	493.3	mA
		WCDMA B1 HSUPA @22.56dBm	493.3	mA
		WCDMA B8 HSDPA @23.37dBm	439.7	mA
		WCDMA B8 HSUPA @22.79dBm	443.6	mA
	GSM voice call	EGSM900 PCL=5 @32.52dBm	258.9	mA
		EGSM900 PCL=12 @19.27dBm	126.0	mA

		EGSM900 PCL=19 @5.34dBm	96.7	mA
		DCS1800 PCL=0 @29.33dBm	199.3	mA
		DCS1800 PCL=7 @16.11dBm	112.9	mA
		DCS1800 PCL=15 @1.34dBm	94.0	mA
	WCDMA voice call	WCDMA B1 @23.24dBm	492.9	mA
		WCDMA B8 @22.93dBm	438.3	mA

Table 31: UC200T-GL Current Consumption

Parameter	Description	Condition	Typical	Unit
I_{VBAT}	Power off	Module power off	17	uA
	Sleep mode	**AT+CFUN=0** (USB disconnected)	1.10	mA
		EGSM900 @DRX=2 (USB disconnected)	2.83	mA
		EGSM900 @DRX=5 (USB disconnected)	1.80	mA
		EGSM900 @DRX=5 (USB suspend)	2.00	mA
		EGSM900 @DRX=9 (USB disconnected)	1.48	mA
		DCS1800 @DRX=2 (USB disconnected)	2.76	mA
		DCS1800 @DRX=5 (USB disconnected)	1.77	mA
		DCS1800 @DRX=5 (USB suspend)	1.93	mA
		DCS1800 @DRX=9 (USB disconnected)	1.46	mA
		WCDMA @PF=64 (USB disconnected)	4.50	mA
		WCDMA @PF=64 (USB suspend)	4.60	mA
		WCDMA @PF=128 (USB disconnected)	3.00	mA
		WCDMA @PF=256 (USB disconnected)	2.14	mA

		WCDMA @ PF=512 (USB disconnected)	1.75	mA
	Idle mode	GSM @DRX=5 (USB disconnected)	31.67	mA
		GSM @DRX=5 (USB connected)	28.71	mA
		WCDMA @PF=64 (USB disconnected)	33.89	mA
		WCDMA @PF=64 (USB connected)	30.95	mA
	GPRS data transfer	EGSM900 4DL/1UL @32.97dBm	272.6	mA
		EGSM900 3DL/2UL @32.7dBm	451.1	mA
		EGSM900 2DL/3UL @31.19dBm	536.0	mA
		EGSM900 1DL/4UL @28.95dBm	560.7	mA
		DCS1800 4DL/1UL @29.89dBm	211.0	mA
		DCS1800 3DL/2UL @29.71dBm	326.4	mA
		DCS1800 2DL/3UL @28.18dBm	389.7	mA
		DCS1800 1DL/4UL @26.05dBm	406.0	mA
	EDGE data transfer	EGSM900 4DL/1UL @27.05dBm	202.6	mA
		EGSM900 3DL/2UL @26.89dBm	316.8	mA
		EGSM900 2DL/3UL @24.96dBm	411.4	mA
		EGSM900 1DL/4UL @22.93dBm	494.4	mA
		DCS1800 4DL/1UL @25.67dBm	189.8	mA
		DCS1800 3DL/2UL @25.8dBm	288.7	mA
		DCS1800 2DL/3UL @24.01dBm	367.8	mA
		DCS1800 1DL/4UL @22.17dBm	429.6	mA
	WCDMA data transfer	WCDMA B1 HSDPA @23.68dBm	527.9	mA
		WCDMA B1 HSUPA @22.51dBm	509.7	mA
		WCDMA B2 HSDPA @23.29dBm	502.8	mA

		WCDMA B2 HSUPA @22.18dBm	483.5	mA
		WCDMA B5 HSDPA @22.82dBm	454.1	mA
		WCDMA B5 HSUPA @21.81dBm	442.6	mA
		WCDMA B6 HSDPA @22.96dBm	458.9	mA
		WCDMA B6 HSUPA @22.62dBm	465.3	mA
		WCDMA B8 HSDPA @22.96dBm	474.4	mA
		WCDMA B8 HSUPA @22.04dBm	463.3	mA
	GSM voice call	EGSM900PCL=5 @32.92dBm	266.5	mA
		EGSM900PCL=12 @19.54dBm	124.6	mA
		EGSM900PCL=19 @5.27dBm	94.4	mA
		DCS1800 PCL=0 @29.9dBm	199.2	mA
		DCS1800 PCL=7 @16.61dBm	110.5	mA
		DCS1800 PCL=15 @0.33dBm	90.8	mA
	WCDMA voice call	WCDMA B1 @23.63dBm	520.2	mA
		WCDMA B2 @23.47dBm	496.5	mA
		WCDMA B5 @ 22.91dBm	450.0	mA
		WCDMA B6 @ 23.3dBm	465.2	mA
		WCDMA B8 @ 22.96dBm	474.4	mA

5.5. RF Output Power

The following table shows the RF output power of UC200T module.

Table 32: RF Output Power

Frequency	Max.	Min.
GSM850/EGSM900	33dBm±2dB	5dBm±5dB
DCS1800/PCS1900	30dBm±2dB	0dBm±5dB
GSM850/EGSM900 (8-PSK)	27dBm±3dB	5dBm±5dB
DCS1800/PCS1900 (8-PSK)	26dBm±3dB	0dBm±5dB
WCDMA B1/B2/B5/B6/B8	24dBm+1/-3dB	<-49dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 4.0dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

5.6. RF Receiving Sensitivity

The RF receiving sensitivity of UC200T is listed in the following tables.

Table 33: UC200T-EM Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO[1)]	3GPP
EGSM900	-109.5dBm	NA	NA	-102.4dBm
DCS1800	-109dBm	NA	NA	-102.4dBm
WCDMA B1	-110dBm	NA	NA	-106.7dBm
WCDMA B8	-110dBm	NA	NA	-103.7dBm

Table 34：UC200T-GL Conducted RF Receiving Sensitivity

Frequency	Receive sensitivity			
	Primary	Diversity	SIMO	3GPP（SIMO）
GSM850	-109.5dBm	NA	NA	-102.4dBm
EGSM900	-109.5dBm	NA	NA	-102.4dBm
DCS1800	-108.5dBm	NA	NA	-102.4dBm
PCS1900	-108dBm	NA	NA	-102.4dBm
WCDMA B1	-109.5dBm	NA	NA	-106.7dBm
WCDMA B2	-109.5dBm	NA	NA	-104.7dBm
WCDMA B5	-110dBm	NA	NA	-104.7dBm
WCDMA B6	-111dBm	NA	NA	-106.7dBm
WCDMA B8	-110dBm	NA	NA	-103.7dBm

5.7. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling, and operation of any application that incorporates the module.

The following table shows the module electrostatics discharge characteristics.

Table 35: Electrostatics Discharge Characteristics (Temperature=25 ºC, Humidity=45%)

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±8	±12	kV
All Antenna Interfaces	±8	±12	kV
Other Interfaces	±0.5	±1	kV

6 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.05mm unless otherwise specified.

6.1. Mechanical Dimensions of the Module

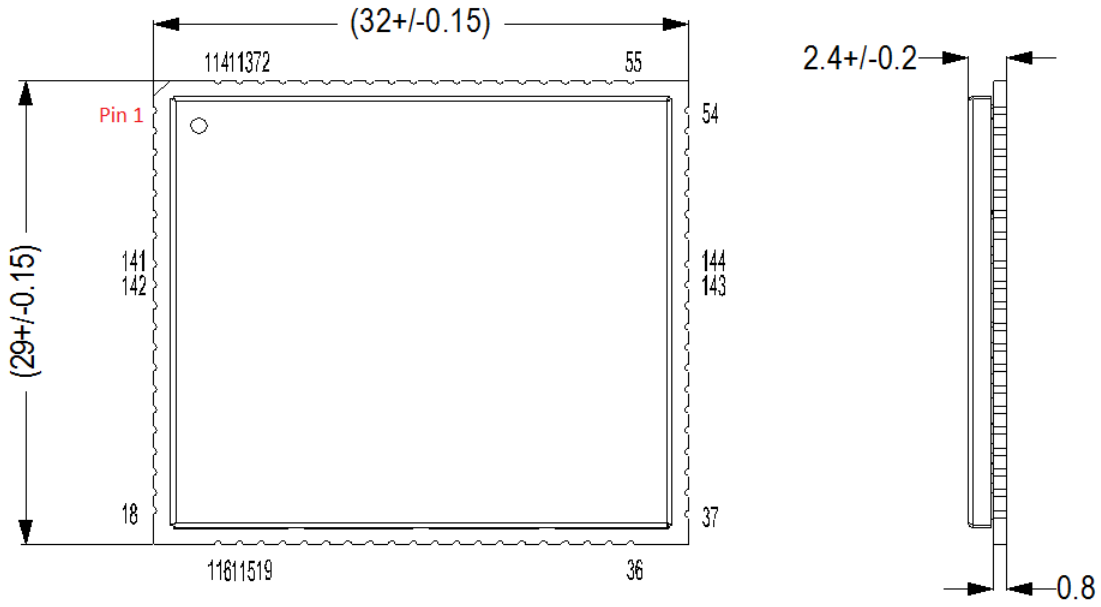


Figure 37: Module Top and Side Dimensions

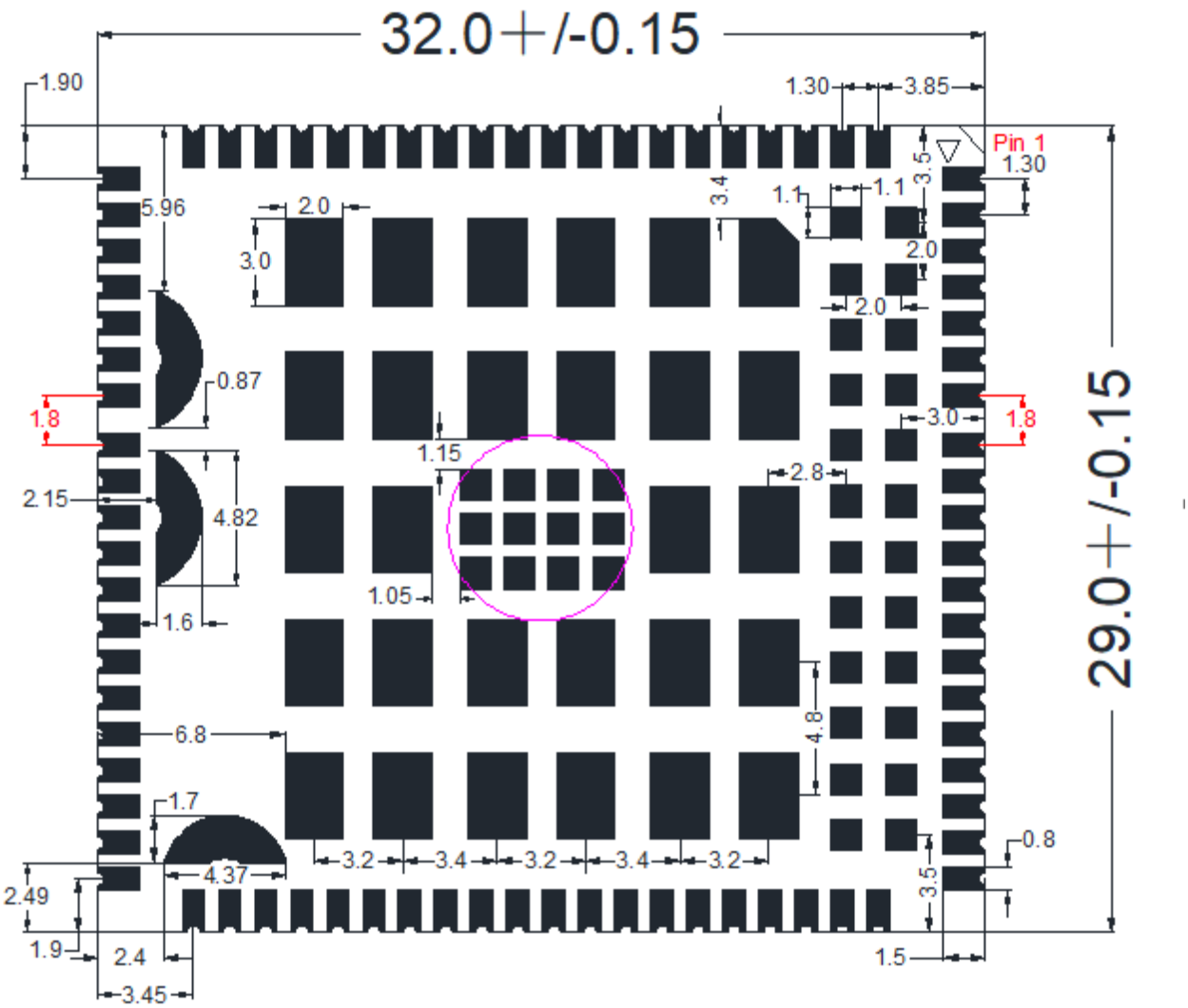


Figure 38: Module Bottom Dimensions (Bottom View)

6.2. Recommended Footprint

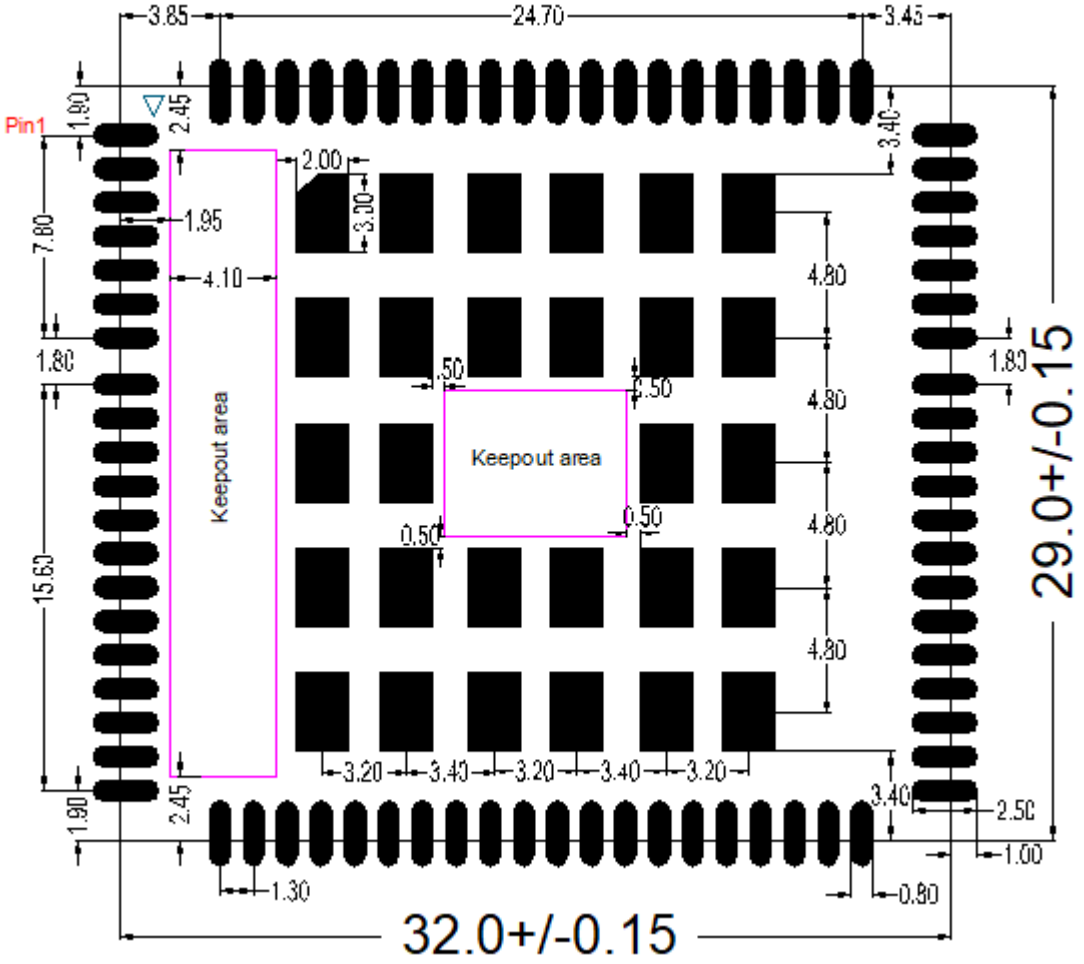


Figure 39: Recommended Footprint (Top View)

NOTES

1. Pins 73~84 and 117~140 included in the keepout area should not be used when designing schematics and PCB layout.
2. For easy maintenance of the module, please keep about 3mm between the module and other components in the host PCB.

6.3. Top and Bottom View of UC200T

Figure 40: Top View of the Module

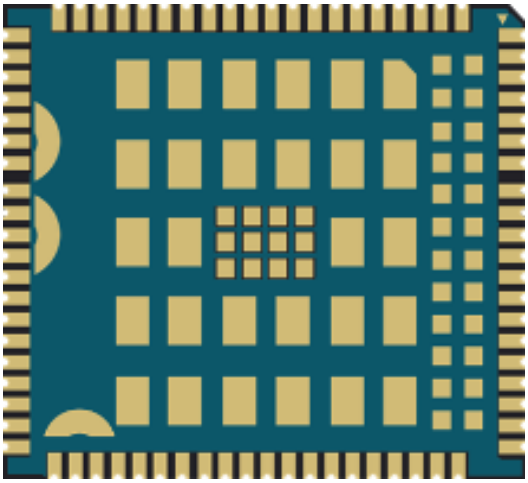


Figure 41: Bottom View of the Module

NOTE

These are renderings of UC200T module. For authentic appearance, please refer to the module that you receive from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage

UC200T is stored in a vacuum-sealed bag. It is rated at MSL 3, and its storage restrictions are listed below .

1. Shelf life in a vacuum-sealed bag: 12 months at <40ºC/90%RH.

2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high-temperature processes must be:

   - Mounted within 168 hours at the factory environment of ≤30ºC/60%RH.
   - Stored at <10% RH.

3. Devices require baking before mounting if any circumstances below occurs:

   - When the ambient temperature is 23ºC±5ºC and the humidity indicator card shows the humidity is>10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤30ºC/60%RH.

4. If baking is required, devices may be baked for 8 hours at 120ºC±5ºC.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (120ºC) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for the baking procedure.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18mm~0.20mm. For more details, please refer to ***document [1]***.

It is suggested that the peak reflow temperature is 238ºC~245ºC, and the absolute maximum reflow temperature is 245ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

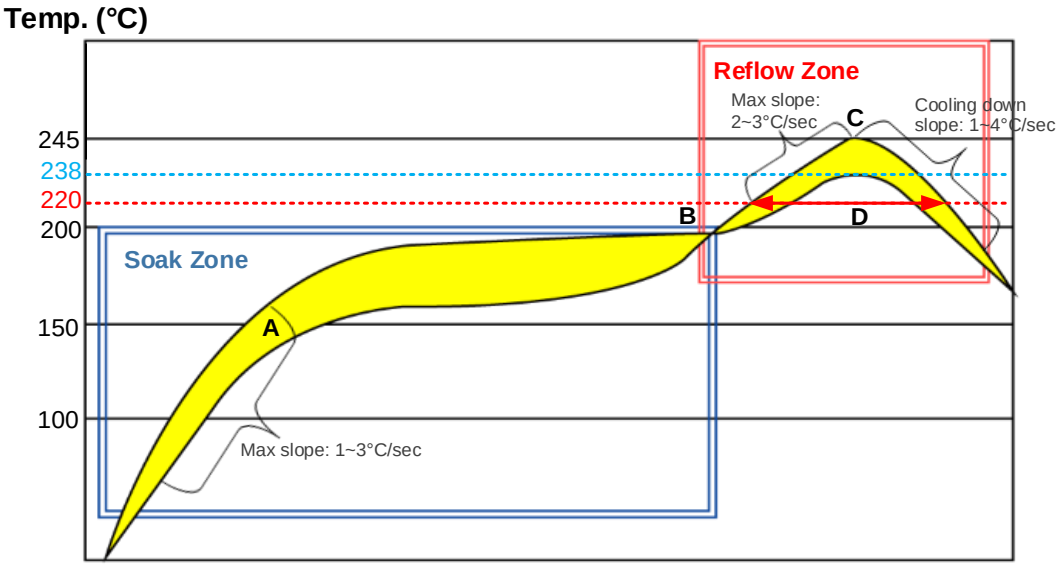


Figure 42: Reflow Soldering Thermal Profile

Table 36: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1°C/sec ~ 3°C/sec
Soak time (between A and B: 150°C and 200°C)	60 sec ~ 120 sec
Reflow Zone	
Max slope	2°C/sec ~ 3°C/sec

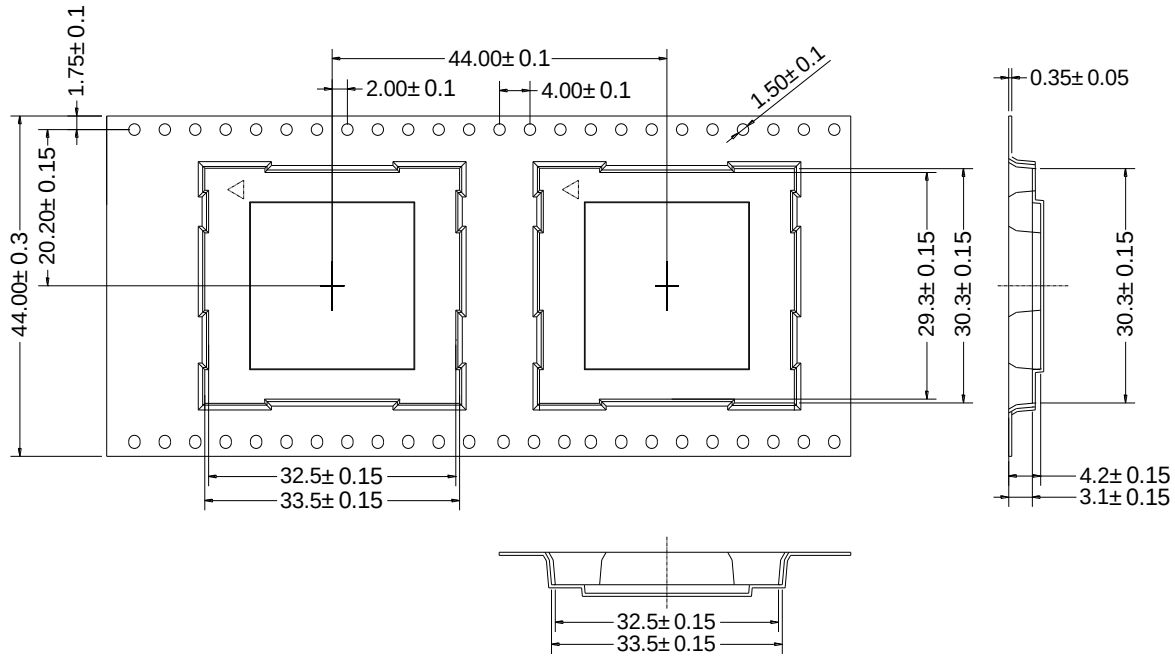
Reflow time (D: over 220°C)	40 sec ~ 60 sec
Max temperature	238°C ~ 245°C
Cooling down slope	1°C/sec ~ 4°C/sec
Reflow Cycle	
Max reflow cycle	1

NOTES

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the 2D barcode is still readable, although white rust may be found.

7.3. Packaging

UC200T is packaged in tape and reel carriers. Each reel is 330mm in diameter, each tape is 11.88m in length and contains 250pcs modules. The detailed package information is shown below (measured in mm).



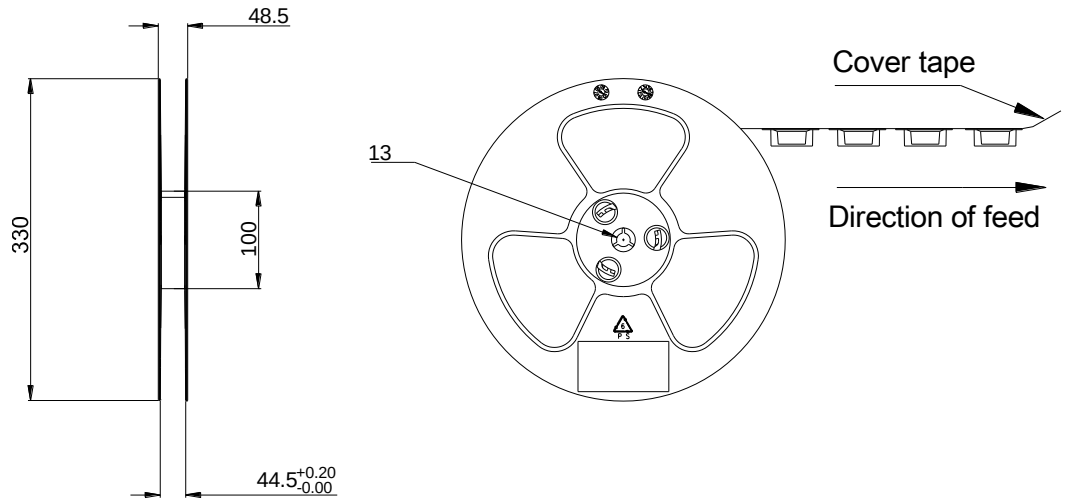


Figure 43: Tape and Reel Specifications

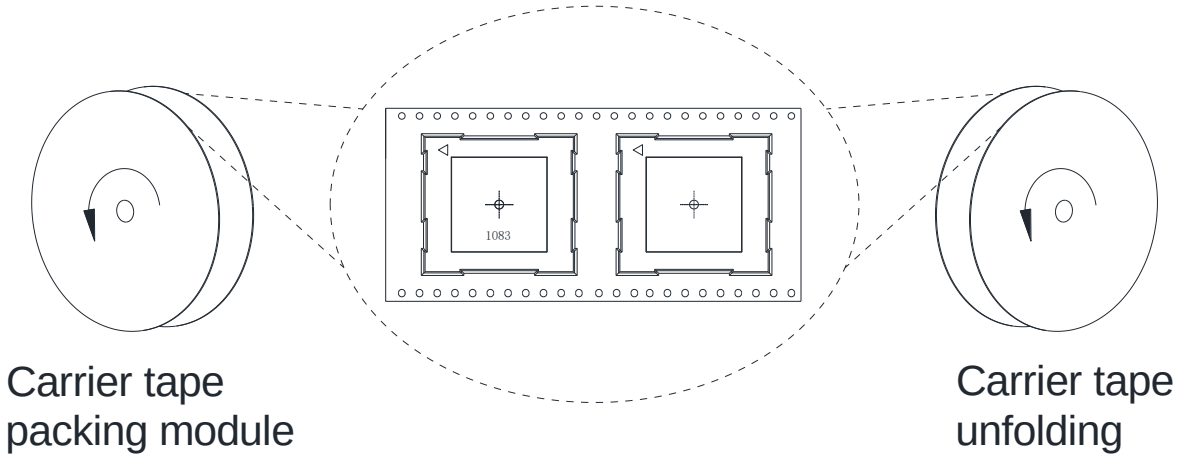


Figure 44: Tape and Reel Directions

8 Appendix A References

Table 37: Related Documents

SN	Document Name	Remark
[1]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[2]	Quectel_UC200T_AT_Commands_Manual	UC200T AT Commands Manual
[3]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[4]	Quectel_UMTS&LTE_EVB_User_Guide	UMTS&LTE EVB user guide for UMTS&LTE modules

Table 38: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear To Send
DL	Downlink
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
EGSM	Enhanced GSM

ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
FDD	Frequency Division Duplex
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP-over-SSL
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	Hypertext Transfer Protocol
LED	Light Emitting Diode
ME	Mobile Equipment
LTE	Long Term Evolution
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Level
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PF	Paging Frame

PPP	Point-to-Point Protocol
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver &Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value

V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

9 Appendix B GPRS Coding Schemes

Table 39: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

10 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 40: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5

13	3	3	NA
14	4	4	NA
15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

11 Appendix D EDGE Modulation and Coding Schemes

Table 41: EDGE Modulation and Coding Schemes

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1:	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2:	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3:	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4:	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps